BAB V

KESIMPULAN

5.1 KESIMPULAN

Dari proses perencanaan sampai dengan tahap pengujian serta hasil pengukuran yang telah dilakukan, dapat diambil beberapa kesimpulan sebagai berikut:

1. Dari hasil pengujian terlihat bahwa sistem kontrol yang memanfaatkan jaringan telepon sebagai media transmisinya bekerja dengan baik sesuai dengan tujuan yang ingin dicapai.
2. Sinyal DTMF yang dibangkitkan oleh pesawat telepon jenis tekan (dial tone) dapat dipergunakan sebagai masukan dari rangkaian pengendali.
3. Sistem kontrol ini cukup baik walaupun mempunyai ketergantungan pada pesawat telepon dan jaringannya.

DAFTAR PUSTAKA

1. Barry Woollard, Elektronika Praktis, terj. H. Kristono, Jakarta : Pradnya Paramita, 1988.
2. H.M.E., Institut Teknologi Bandung, Pengantar Teknik Digital Teori dan Praktek, Bandung ; Majalah Elektron, 1988.
3. Malvino, Paul Albert, Digital Computer Electronics, edisi kedua, terj. Tjia May On, Jakarta : Erlangga, 1988.
4. Malvino, Paul Albert, Prinsip-prinsip Elektroniks, Jakarta : 1988.
5. Millman, Jacob, Aproksimasi Rangkaian Semi Konduktor, edisi kedua, terj. Tjia May On, Jakarta : Erlangga, 1986.
6. PT. Telkom, FTP TELKOM 92, edisi kedua : PT. TELKOM.
7. Robert F., Couglin, Operational Amplifier and Linier Integerated Circuit, prentice: Hall International, 1982.

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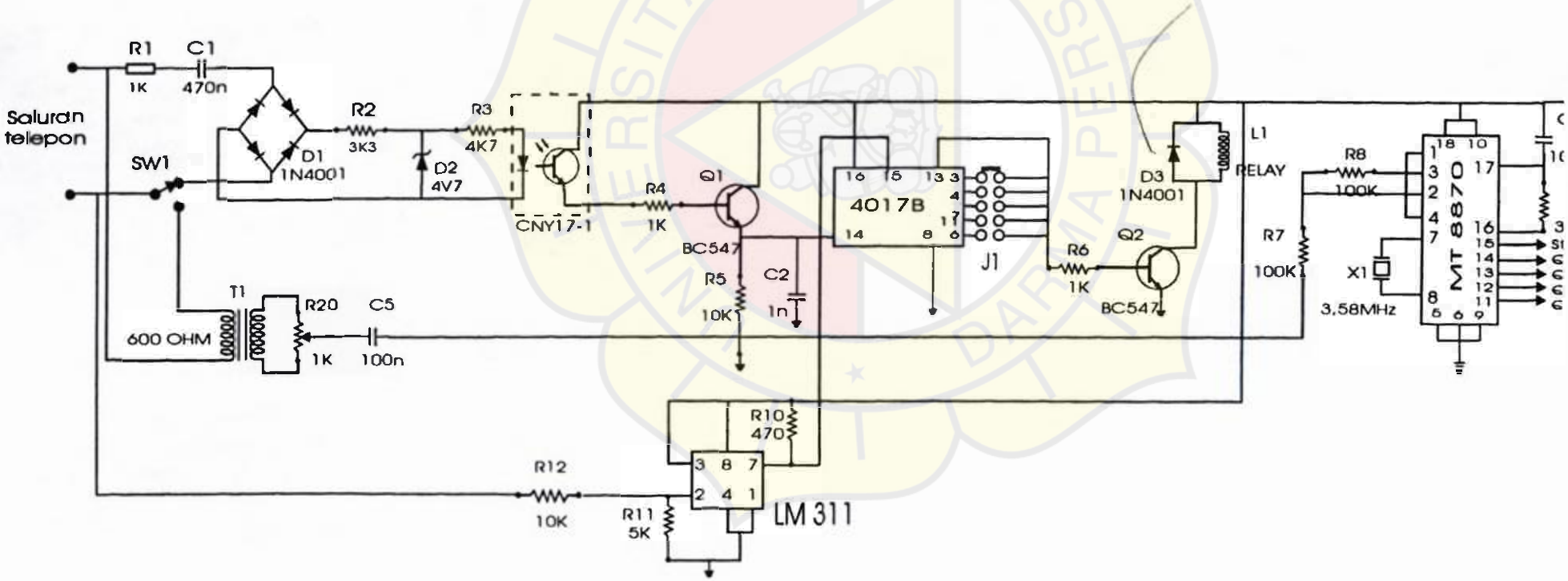
		Tamat tahun 1992
		4. Universitas Darma Persada Jakarta
		Tamat tahun 199

Jakarta, 17 Agustus 1997

(Nur Wahyu Diantoro)

LAMPIRAN-LAMPIRAN


R1
C1
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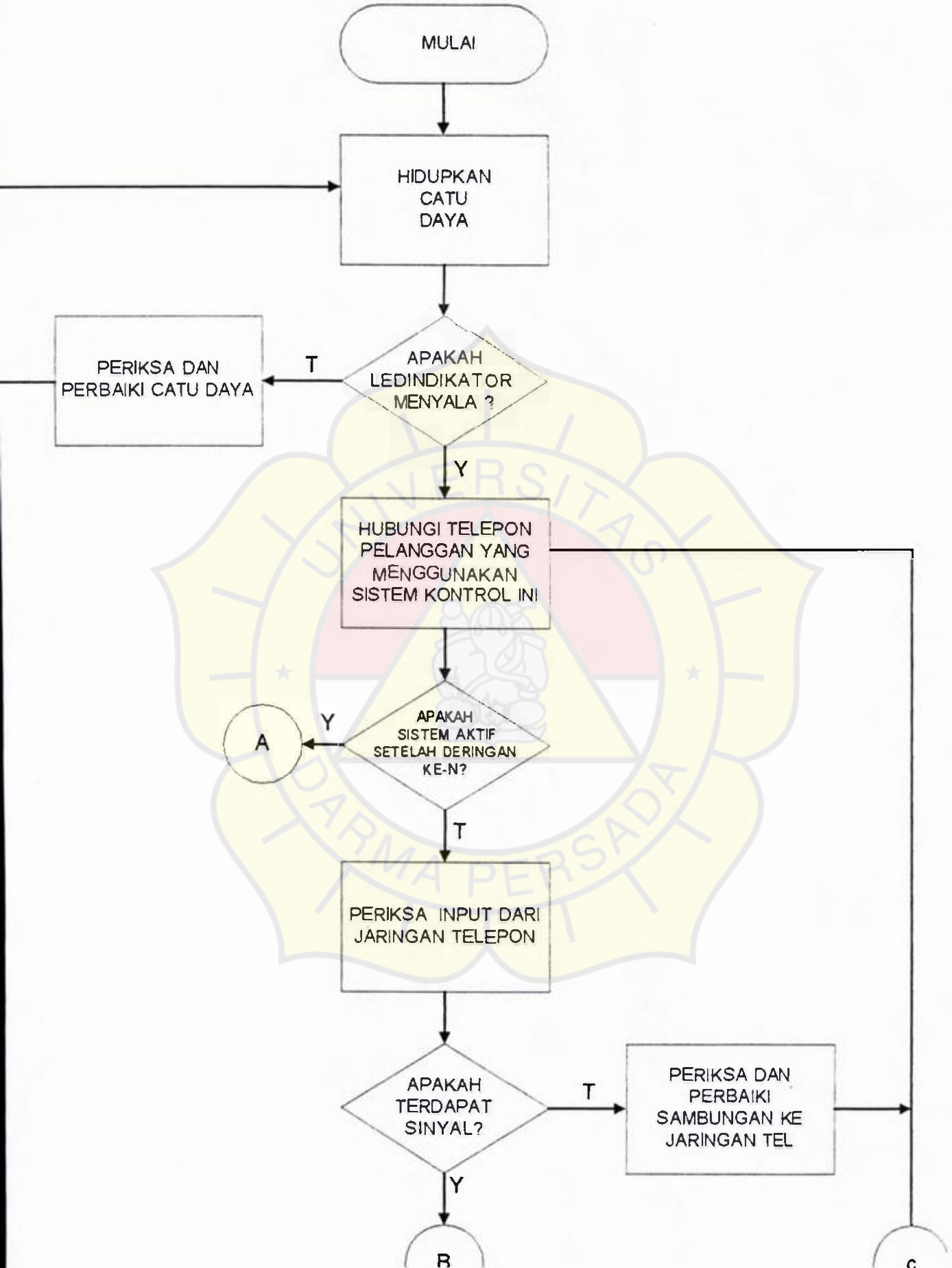
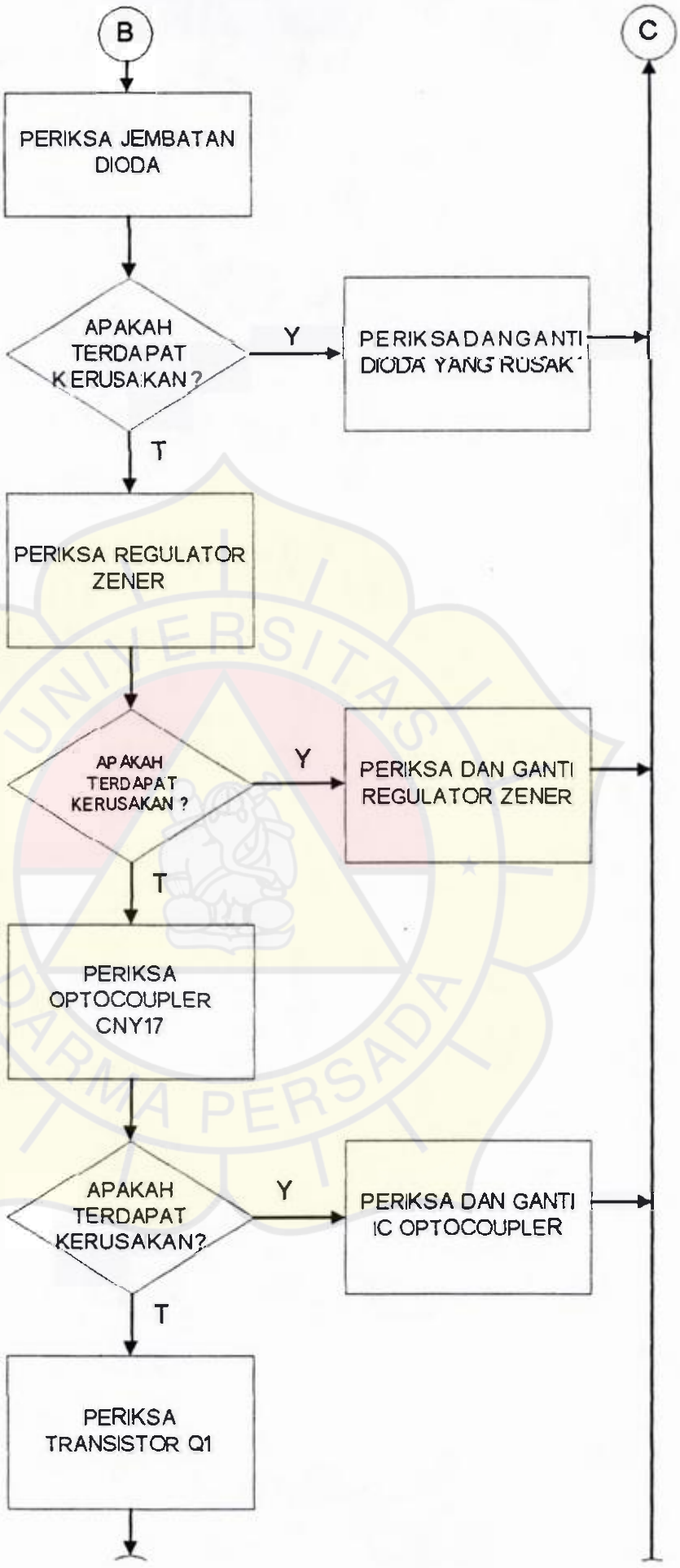
Saluran telepon
SW1
D1
1N4001
R2
3K3
R3
4K7
D2
4V7
CNY17-1
R4
1K
Q1
BC547
R5
10K
C2
1n
4017B
J1
D3
1N4001
L1
RELAY
Q2
BC547
R6
1K
R7
100K
R8
100K
X1
3,58MHz
MT 8870
T1
600 OHM
R20
1K
C5
100n
R10
470
R12
10K
R11
5K
LM 311

)K ANTAR MUKA JARINGAN TELEPON




B
C
PERIKSA JEMBATAN DIODA
APAKAH TERDAPAT KERUSAKAN ?
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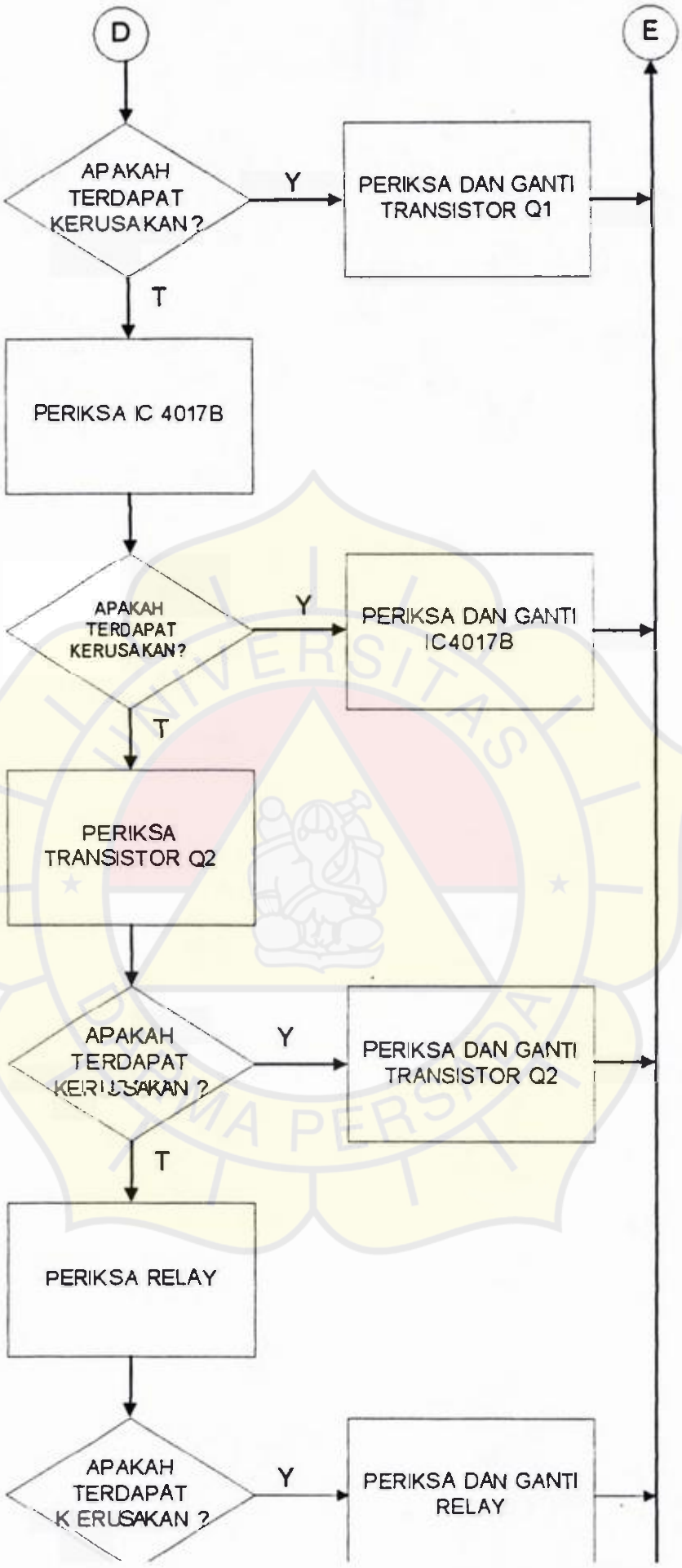
PERIKSA DAN GANTI DIODA YANG RUSAK
T
PERIKSA REGULATOR ZENER
APAKAH TERDAPAT KERUSAKAN ?
Y
PERIKSA DAN GANTI REGULATOR ZENER
T
PERIKSA OPTOCOUPLER CNY17
APAKAH TERDAPAT KERUSAKAN?
Y
PERIKSA DAN GANTI IC OPTOCOUPLER
T
PERIKSA TRANSISTOR Q1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E
APAKAH TERDAPAT KERUSAKAN?
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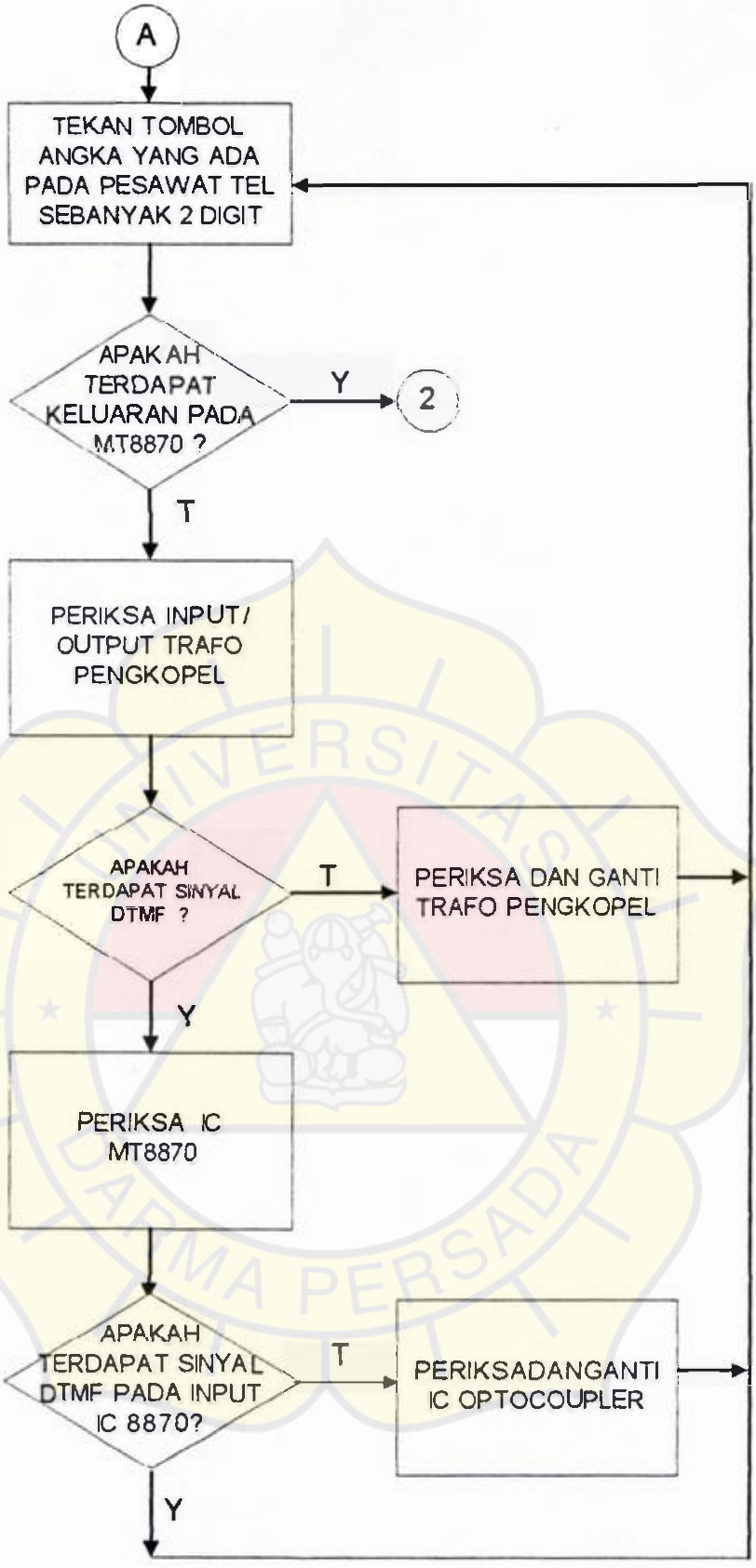
PERIKSA DAN GANTI TRANSISTOR Q1
T
PERIKSA IC 4017B
APAKAH TERDAPAT KERUSAKAN?
Y
PERIKSA DAN GANTI IC4017B
T
PERIKSA TRANSISTOR Q2
APAKAH TERDAPAT KERUSAKAN ?
Y
PERIKSA DAN GANTI TRANSISTOR Q2
T
PERIKSA RELAY
APAKAH TERDAPAT KERUSAKAN ?
Y
PERIKSA DAN GANTI RELAY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TEKAN TOMBOL ANGKA YANG ADA PADA PESAWAT TEL SEBANYAK 2 DIGIT
APAKAH TERDAPAT KELUARAN PADA MT8870 ?
Y
2
T
PERIKSA INPUT/ OUTPUT TRAFO PENGKOPEL
APAKAH TERDAPAT SINYAL DTMF ?
T
PERIKSA DAN GANTI TRAFO PENGKOPEL
Y
PERIKSA IC MT8870
APAKAH TERDAPAT SINYAL DTMF PADA INPUT IC 8870?
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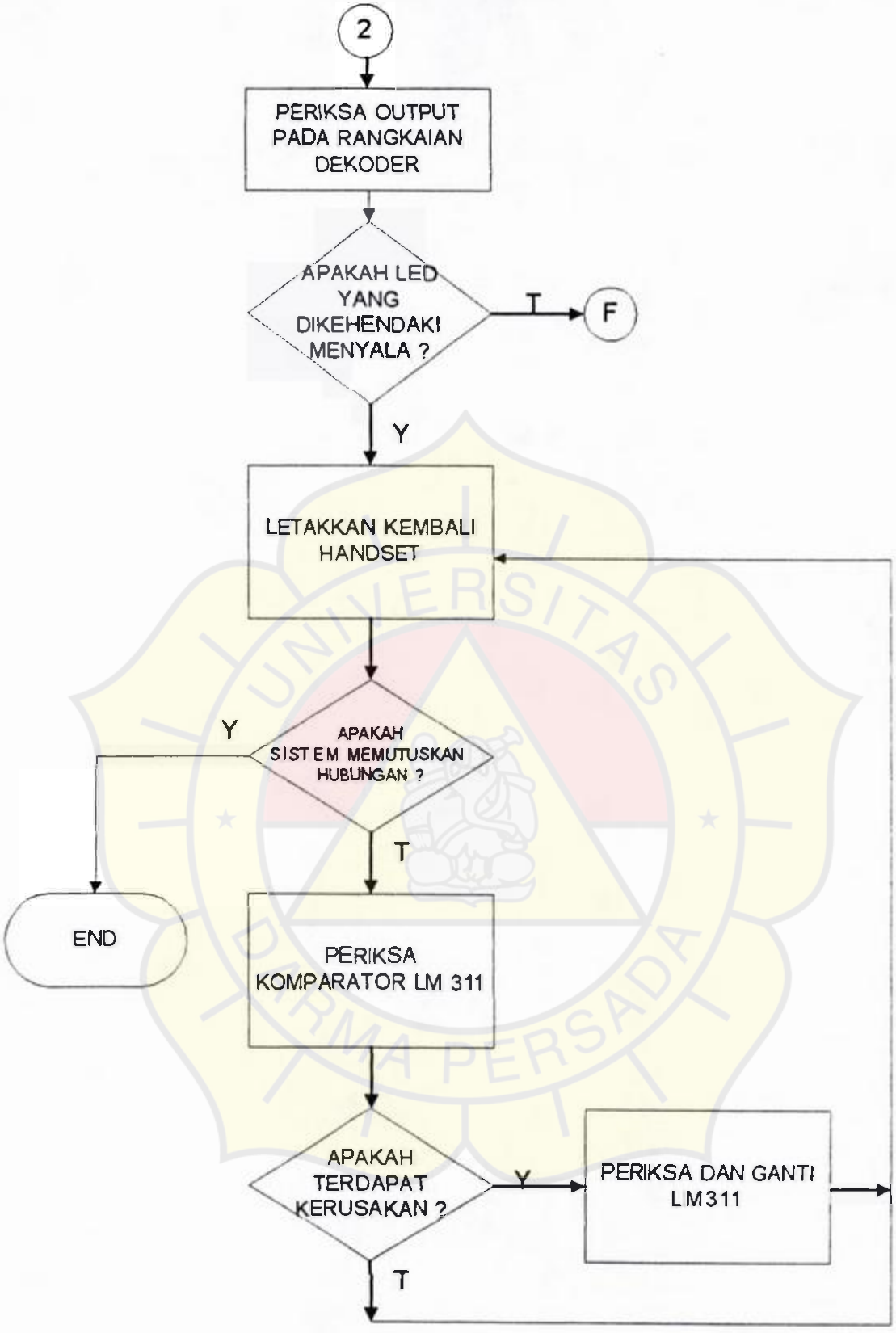
PERIKSADANGANTI IC OPTOCOUPLER
Y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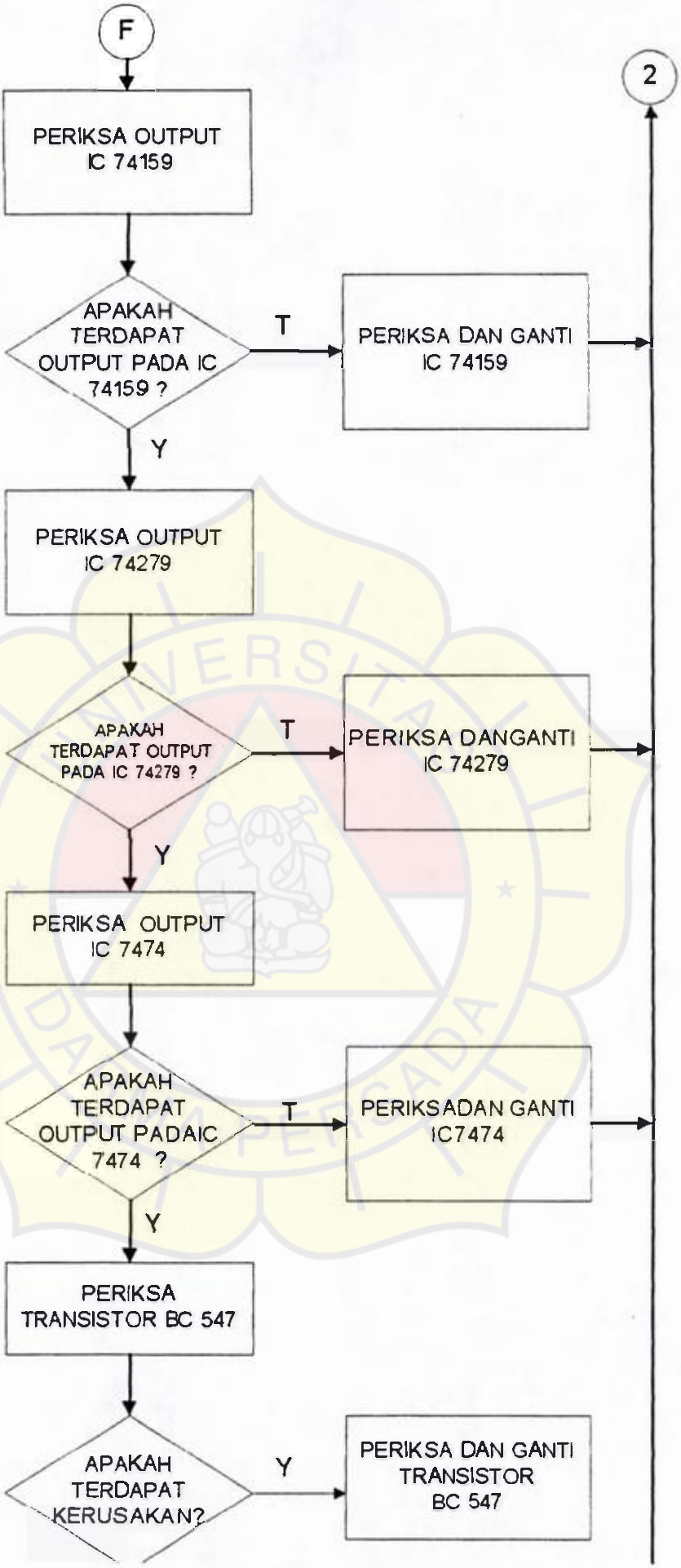
PERIKSA OUTPUT PADA RANGKAIAN DEKODER
APAKAH LED YANG DIKEHENDAKI MENYALA ?
T
F
Y
LETAKKAN KEMBALI HANDSET
Y
APAKAH SISTEM MEMUTUSKAN HUBUNGAN ?
T
END
PERIKSA KOMPARATOR LM 311
APAKAH TERDAPAT KERUSAKAN ?
Y
PERIKSA DAN GANTI LM311
T

BLOK RANGKAIAN PENGENDALI



National Semiconductor

Voltage Comparators

LM311 voltage comparator

general description

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

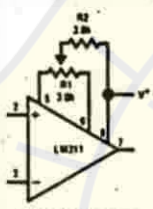
features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C. See the "application hints" of the LM311 for application help.

auxiliary circuits*

*Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.

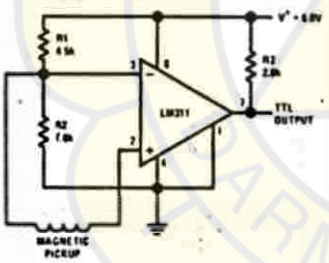


Offset Balancing

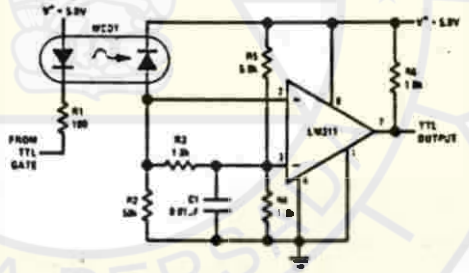
Strobing

Increasing Input Stage Current*

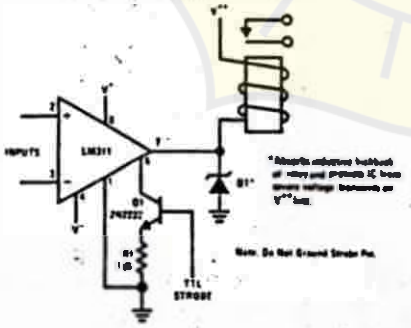
typical applications*



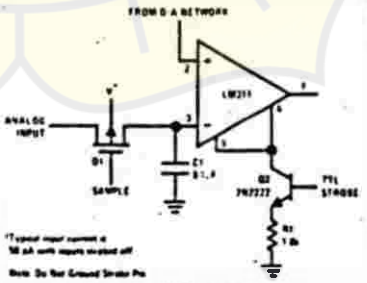
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe



Strobing o f Both Input* and Output Stages

absolute maximum ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Voltage at Strobe Pin	$V^+ - 5$ V

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35$V, $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8, −14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5$ V, $V^- = 0$, $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185° C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2ounce copper conductors. The thermal resistance of the dual-in-line package is 100° C/W, junction to ambient.

Note 3: These specifications apply for V_S = ±15V and the Ground pin at ground, and 0° C<T_A< +70° C, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

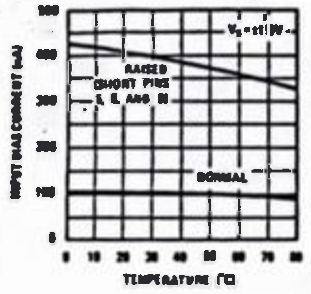
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

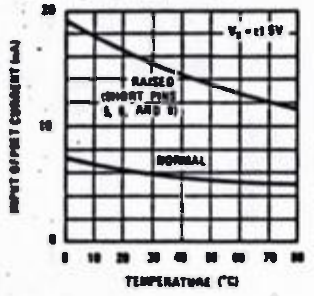
Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

typical performance characteristics

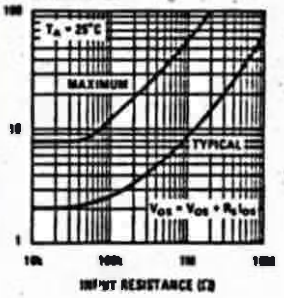
Input Bias Current



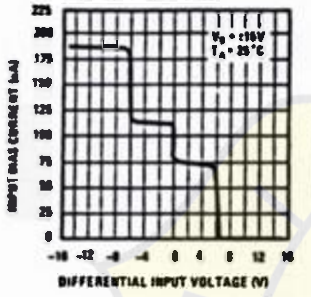
Input Offset Current



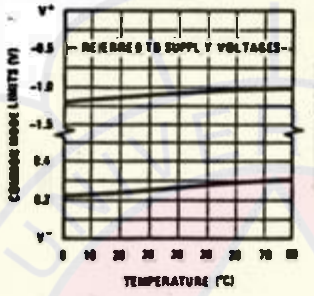
Offset Error



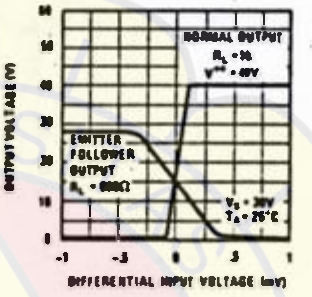
Input Characteristics



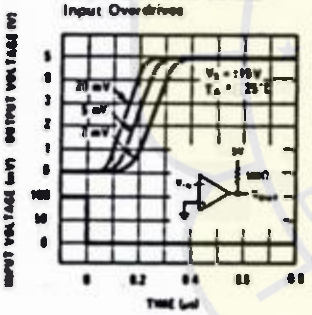
Common Mode Limits



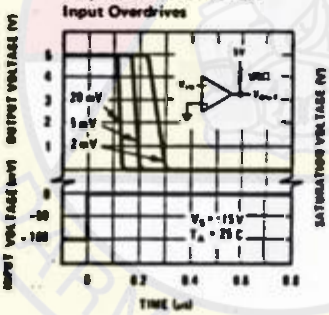
Transfer Function



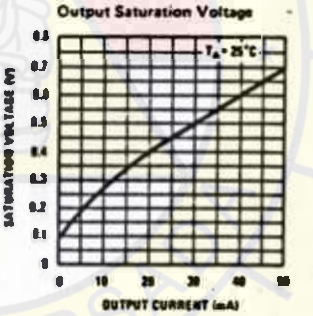
Response Time for Various Input Overdrives



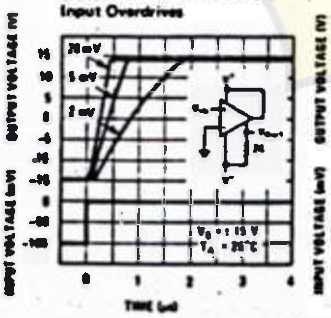
Response Time for Various Input Overdrives



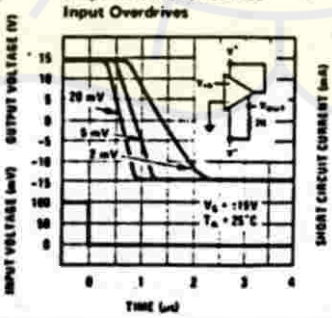
Output Saturation Voltage



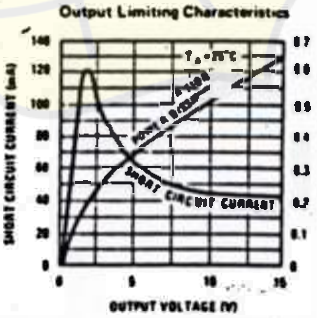
Response Time for Various Input Overdrives



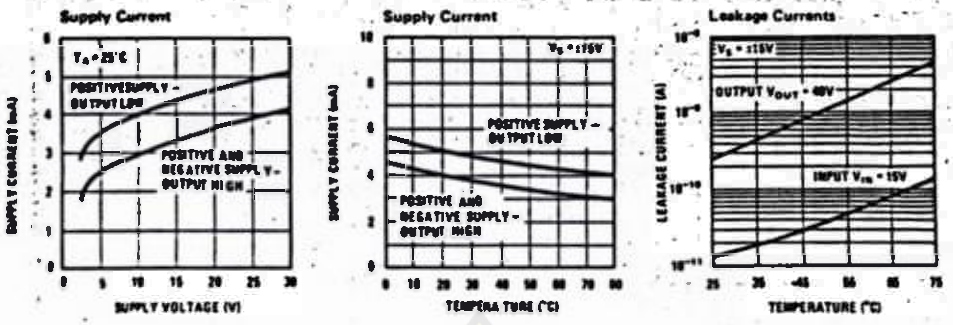
Response Time for Various Input Overdrives



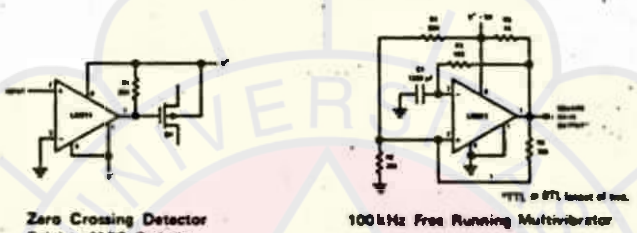
Output Limiting Characteristics



typical performance characteristics (con't)

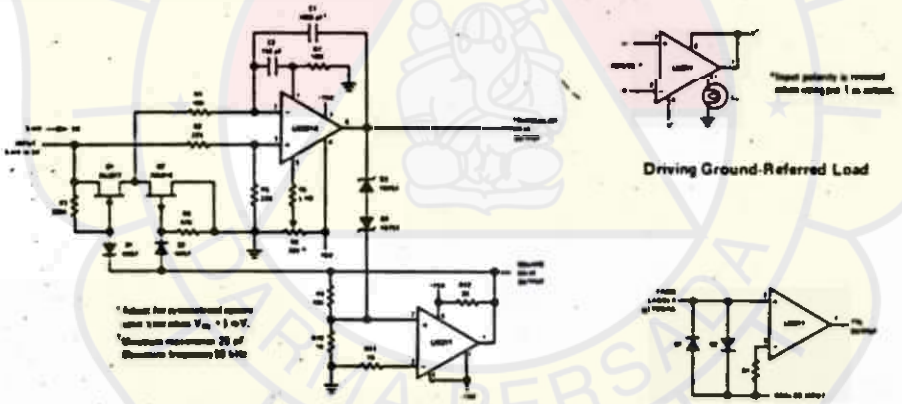


typical applications



Zero Crossing Detector Driving MOS Switch

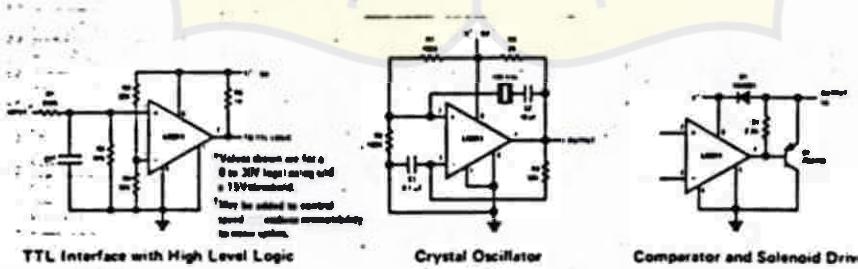
100 kHz Free Running Multivibrator



Driving Ground-Referred Load

10 Hz to 10 kHz Voltage Controlled Oscillator

Using Clamp Diodes to Improve Response

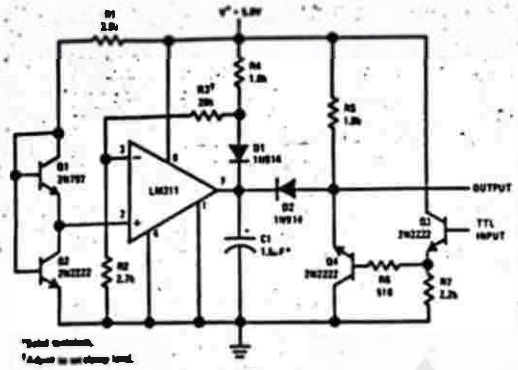


TTL Interface with High Level Logic

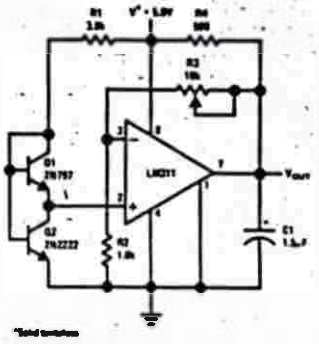
Crystal Oscillator

Comparator and Solenoid Driver

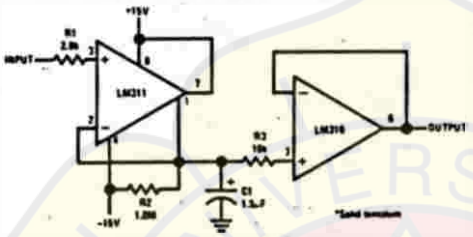
typical applications (con't)



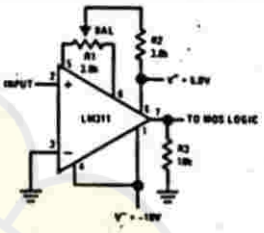
Precision Squarer



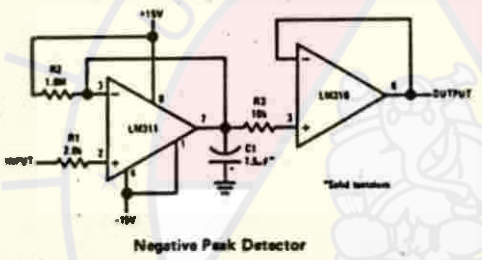
Low Voltage Adjustable Reference Supply



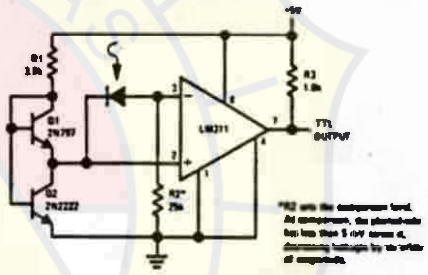
Positive Peak Detector



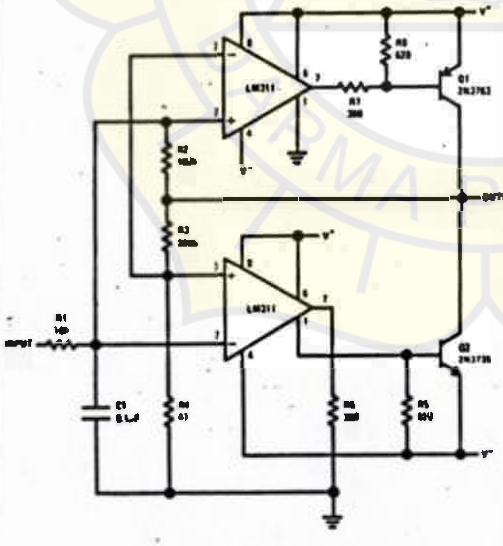
Zero Crossing Detector driving MOS logic



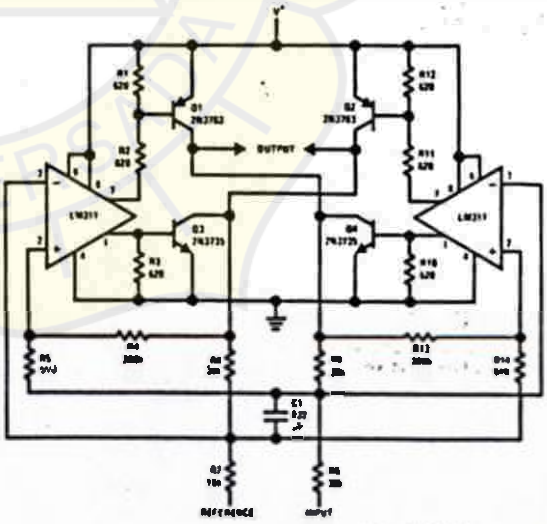
Negative Peak Detector



Precision Photodiode Comparator

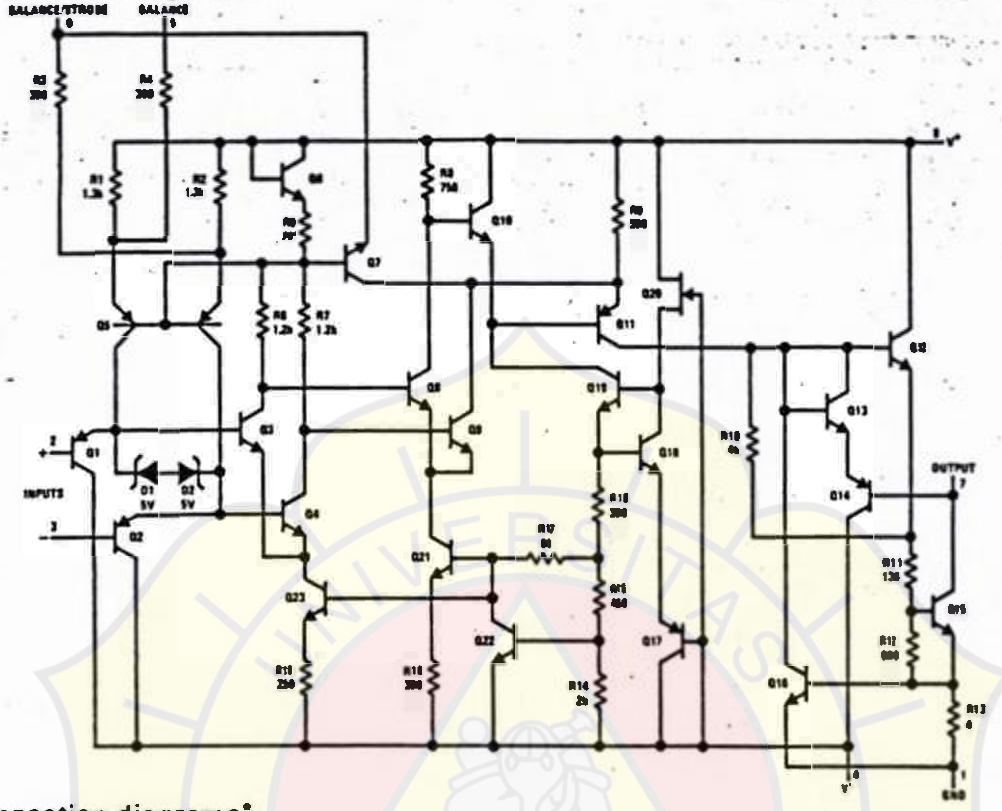


Switching Power Amplifier



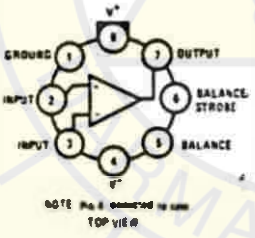
Switching Power Amplifier

schematic diagram



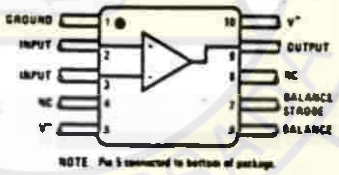
connection diagrams*

Metal Can Package



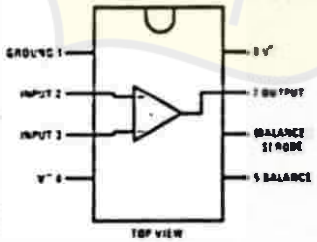
Order Number LM311H
See NS Package H08C

Flat Package



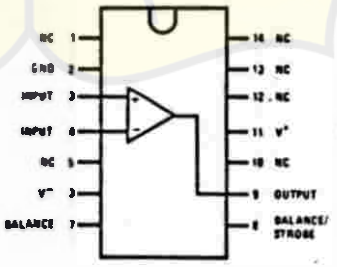
Order Number LM311F
See NS Package F10A

Dual-In-Line Package



Order Number LM311N
See NS Package N08B
Order Number LM311J-8
See NS Package J08A

Dual-In-Line Package



Order Number LM311D
See NS Package D14E
Order Number LM311N-14
See NS Package N14A
Order Number LM311J
See NS Package J14A

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

application hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

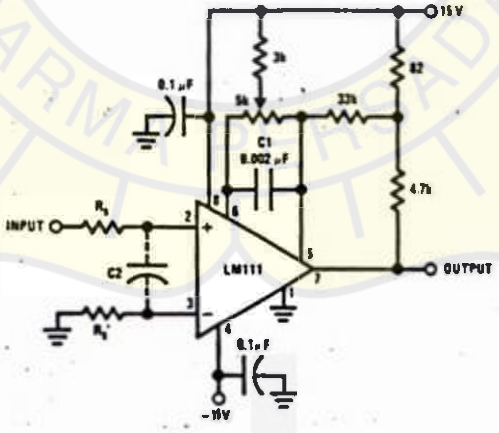
1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.

2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.

3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.

4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



Pin connections shown are for LM111H in 8-lead TO-5 hermetic package

FIGURE 1. Improved Positive Feedback

National Semiconductor

Industrial/Automotive/Functional Blocks/ Telecommunications

LM555/LM555C timer

general description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

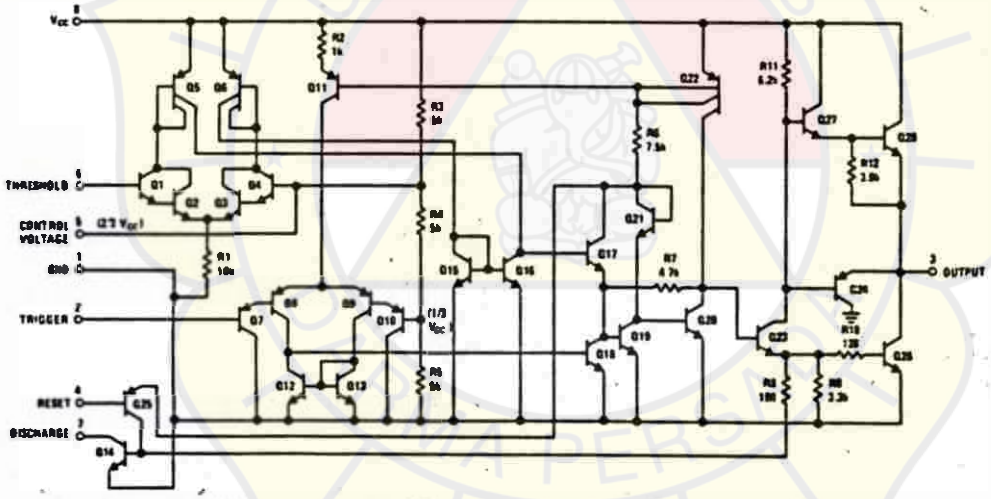
features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

applications

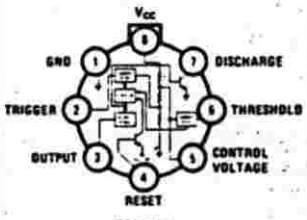
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

schematic diagram



connection diagrams

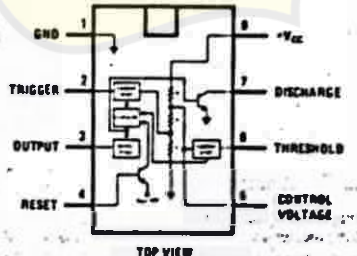
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LM556CN
See NS Package N08B
Order Number LM555J or LM555CJ
See NS Package J08A

absolute maximum ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5	2		1		%
Drift with Temperature	R_A, R_B = 1k to 100k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5	3.0		1.5		%
Drift with Supply			0.05	0.2		0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5	5		2.25	7	%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15	0.2		0.30	0.5	%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

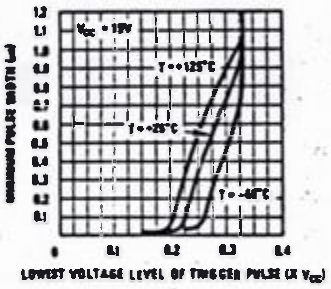
Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: This will determine the maximum value of R_A + R_B for 15V operation. The maximum total (R_A + R_B) is 20 MΩ.

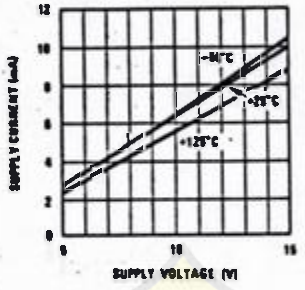
Note 5: No protection against excessive pin 7 currents necessary providing the package dissipation rating will not be exceeded.

typical performance characteristics

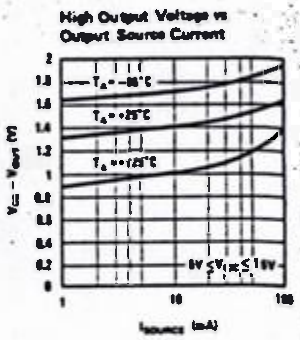
Minimum Pulse Width Required for Triggering



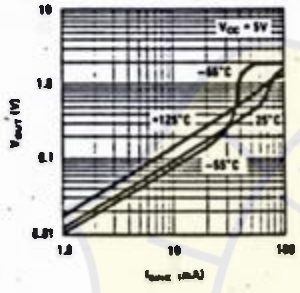
Supply Current vs Supply Voltage



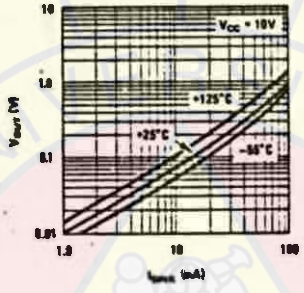
High Output Voltage vs Output Source Current



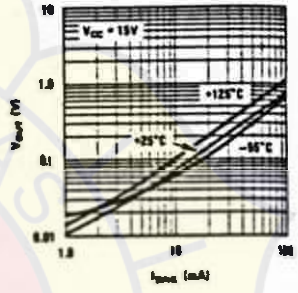
Low Output Voltage vs Output Sink Current



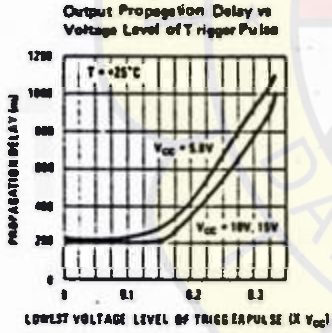
Low Output Voltage vs Output Sink Current



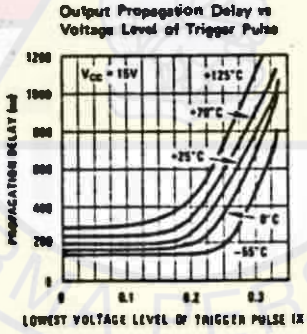
Low Output Voltage vs Output Sink Current



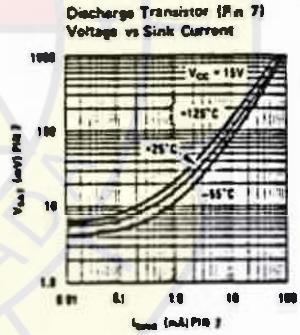
Output Propagation Delay vs Voltage Level of Trigger Pulse



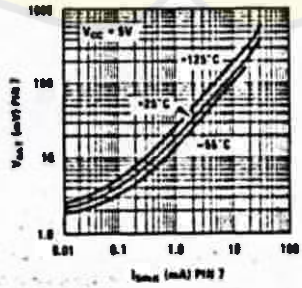
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



applications information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

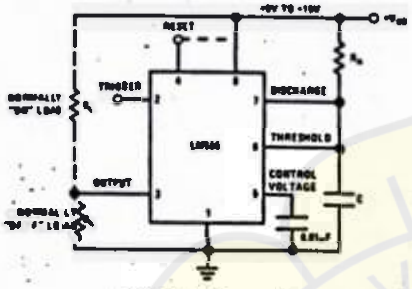


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.

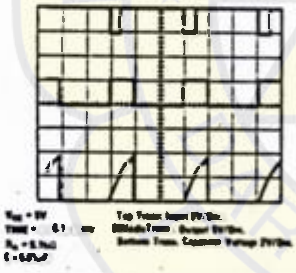


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

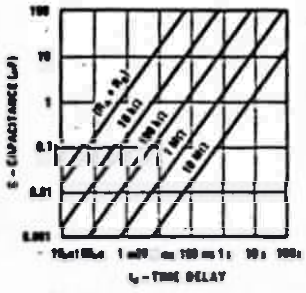


FIGURE 3. Time Delay

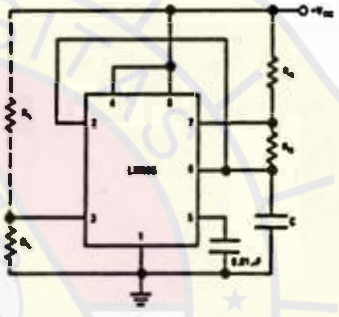


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

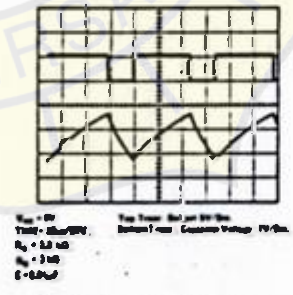


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693(R_A + R_B)C$$

And the discharge time (output low) by:

$$t_2 = 0.693(R_B)C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693(R_A + 2R_B)C$$

applications information (con't)

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $D = \frac{R_B}{R_A + 2R_B}$

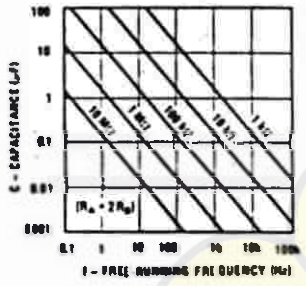


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

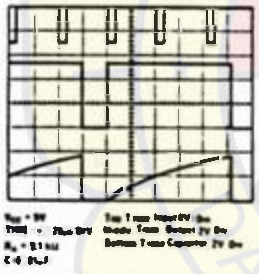


FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

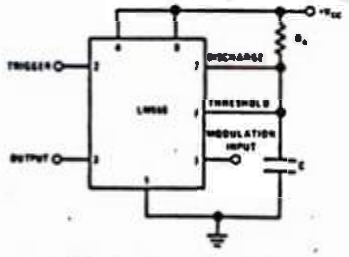


FIGURE 8. Pulse Width Modulator

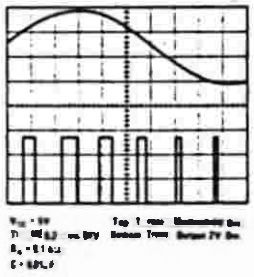


FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

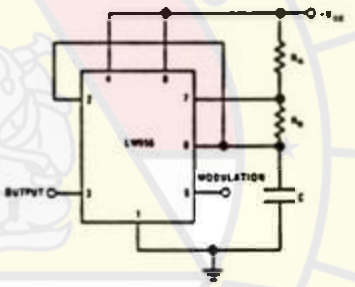


FIGURE 10. Pulse Position Modulator

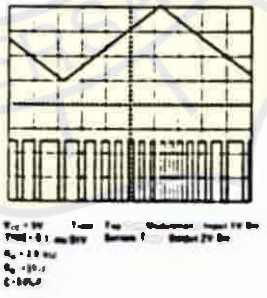


FIGURE 11. Pulse Position Modulator

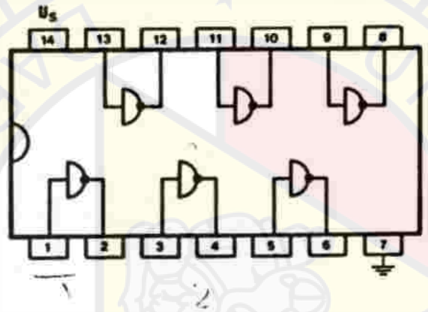
LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is

7404 /1

Inverters with totem-pole outputs

Function table see section 1



7404 /1 T_U = 0...70°C	Type T_U = −25...85°C	Type T_U = −55...125°C	Manufact.	B Bauf.	P_{typ} mW	t_P E→O		t_P E→O (max)		Bem. – Note
FJH 261			Phi,Sig,Val	5a	63	8	12	≤15	≤22	
FLH 211	FLH 216		Sie,Tun	5a	63	8	12	≤15	≤22	
HD 7404			Hit	5a	60	8	13	≤15	≤22	
M 53304			Mit	5a	60	8	13	≤15	≤22	
MB 416			Fui	5a	60	8	12	≤15	≤22	
MIC 7404 J		MIC 5404 J	ITT	6b	63	8	10	≤15	≤22	
MIC 7404 N		MIC 5404 N	ITT	5a	63	8	10	≤15	≤22	
N 7404 A		S 5404 A	Mul,Phi,Sig	5a	63	8	12	≤15	≤22	
N 7404 F		S 5404 F	Mul,Phi,Sig	6b	63	8	12	≤15	≤22	
SN 7404 J		SN 5404 J	Tix	5c	60	8	12	≤15	≤22	
SN 7404 N	SN 8404 N	SN 5404 N	Tix	5a	60	8	12	≤15	≤22	
T 7404 B			SGS	5a	63	8	12	≤15	≤22	
T 7404 D1		T 5404 D2	SGS	6b	63	8	12	≤15	≤22	
TD 3404			Tos	5a	60	8	12	≤15	≤22	
TL 7404 N	TL 8404 N		AEG	5a	63	8	12	≤15	≤22	
U6A 7404 59X		U7A 5404 51X	Fch	5a						
U7A 7404 59X		U7A 5404 51X	Fch	5a						
μPB 226			Nip	5a	60	8	12	≤15	≤22	

7404 /1 T_U = 0...70°C	Type T_U = −25...85°C	Type T_U = −55...125°C	Manufact.	B Bauf.	P_{typ} mW	t_P E→O		t_P E→O (max)		Bem. – Note
H										
N 74H04 A		S 54H04 A	Mul,Phi,Sig	5a	140	6.5	6	≤10	≤13	
N 74H04 F		S 54H04 F	Mul,Phi,Sig	6b	140	6.5	6	≤10	≤13	
SN 74H04 J		SN 54H04 J	Tix	5c	135	6.5	6	≤10	≤10	
SN 74H04 N		SN 54H04 N	Tix	5a	135	6.5	6	≤10	≤10	
L										
SN 74L04 J		SN 54L04 J	Tix	5c	6	31	35	≤60	≤60	
SN 74L04 N	SN 84L04 N	SN 54L04 N	Tix	5a	6	31	35	≤60	≤60	
LS										
HD 74LS04			Hit	5a	12	10	8	≤15	≤15	
SN 74LS04 J		SN 54LS04 J	Tix	5c	12	10	8	≤15	≤15	
SN 74LS04 N		SN 54LS04 N	Tix	5a	12	10	8	≤15	≤15	
SN 74LS04N-10			Tix	5a	12	10	8	≤15	≤15	E: 15V
S										
HD 74S04			Hit	5a	112	3	3	≤5	≤4.5	
MB 604			Mit	5a	112	3	3	≤5	≤4.5	
N 74S04 A		S 54S04 A	Mul,Phi,Sig	5a	112	3	3	≤5	≤4.5	
N 74S04 F		S 54S04 F	Mul,Phi,Sig	6b	112	3	3	≤5	≤4.5	
N 74S04 W		S 54S04 W	Mul,Phi,Sig	15b	112	3	3	≤5	≤4.5	
SN 74S04 J		SN 54S04 J	Tix	5c	112	3	3	≤5	≤4.5	
SN 74S04 N		SN 54S04 N	Tix	5a	112	3	3	≤5	≤4.5	
SN 74S04 W		SN 54S04 W	Tix	15b	112	3	3	≤5	≤4.5	
μPB 2304			Nip	5a	112	3	3	≤5	≤4.5	

7473 T_U = 0...70°C	Type T_U = −25...85°C	T_U = −55...125°C	Manufact.	B Sort	P_{typ} mW	R,T→Q		R,T→Q		f_T MHz	V
LS											
N 74LS73 A			Mul,Phi,Sig	6a	540	150				30	
N 74LS73 F			Mul,Phi,Sig	9b	540	150				30	
SN 74LS73 J		SN 54LS73 J	Tix	6a	20	15	11	520	520	45	
SN 74LS73 N		SN 54LS73 N	Tix	9a	20	15	11	520	520	45	
SN 74LS73 W		SN 54LS73 W	Tix	10b	20	15	11	520	520	45	
9LS73 DC 1)		9LS73 DM 2)	Fch	6b	540	16				45	
9LS73 FC 1)		9LS73 FM 2)	Fch	15d	540	16				45	
9LS73 PC 1)			Fch	9b	540	16				45	
74LS73 DC 1)		54LS73 DM 2)	Fch	6b	540	16				45	
74LS73 FC 1)		54LS73 FM 2)	Fch	15d	540	16				45	
		54LS73 J	Ray	6b	540		11			5min	
74LS73 PC 1)			Fch	9a	540	16				45	
		54LS73 W	Ray	15d	540		11			5min	

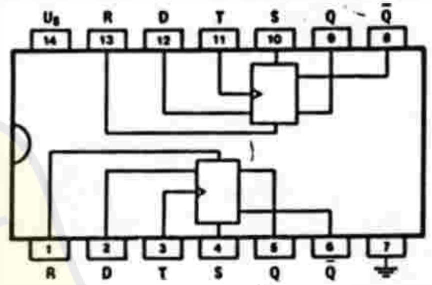
1) FO=8

2) FO=2,5

7474 /1

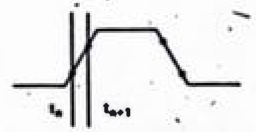
2 D-type flip-flops

Pin	FI N	H	L	LS	S
R	3	2	2	3,3	3
S,T	2	2	2	2,2	2
D	1	1	1	1,1	1



INPUT t_n S	R	D	OUTPUT t_{n+1} Q	$\bar{Q}$
H	L	X	L	H
L	H	X	H	L
L	L	X	*	*
H	H	H	H	L
H	H	L	L	H

*This state is not stable

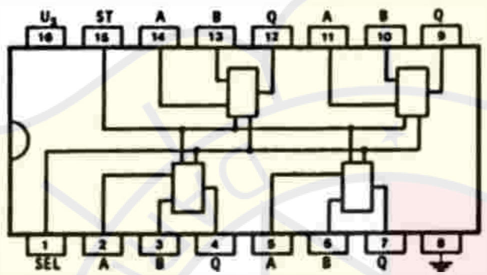


clock pulse

7474 /1 T_U = 0...70°C	Type T_U = −25...85°C	T_U = −55...125°C	Manufact.	B Sort	P_{typ} mW	T→Q		R,S→Q		f_T MHz	V
D 174 C			HFO	6a	70	22	12,5	10,5	8	22	
DM 7474 J		DM 5474 J	Nsc	6b		540				35	
DM 7474 N		DM 5474 N	Nsc	9a		540				35	
FJJ 121			Phi,Sig,Val	6a	86	550				5min	
FLJ 141	FLJ 140		Sie,Tun	9a	86	20	14	540	570	20	
UFB 7474			HTC	6b	86	540		540		5min	
HO 7474			Hit	9a	86		20	540		5min	
IOT 7474 E			Rtz	6a	70	22	12,5	10,5	8	22	
ITT 7474 J		ITT 5474 J	ITT	6c			20			35	
µA 53274			Mit	9a	86		20	540		5min	

74158	4 multiplexers 2 line to 1 line

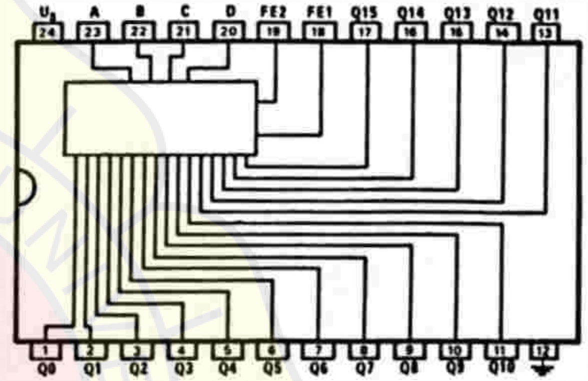
FI (SEL,ST) = 2



INPUT				OUT
ST	SEL	A	B	Q
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

74158	Type		Manufact.	Bauf.	P_{typ}	t_p A,B→Q		t_p A,B→Q		
T_U = 0...70°C	-25...85°C	-55...125°C			mW					
[illegible]			Mo	6a	150	7		9/14		
LS										
SN 74LS158 J		SN 54LS158 J	Ti	6b	120	8				
SN 74LS158 N		SN 54LS158 N	Ti	6a	120	8				
SN 74LS158 W		SN 54LS158 W	Ti	10b	120	8				
S										
SN 74S158 J		SN 54S158 J	Ti	6b	195	4	4	6	6	
SN 74S158 N		SN 54S158 N	Ti	6a	195	4	4	6	6	
SN 74S158 W		SN 54S158 W	Ti	10b	195	4	4	6	6	

74159	4 bit binary decoder with open-collector outputs



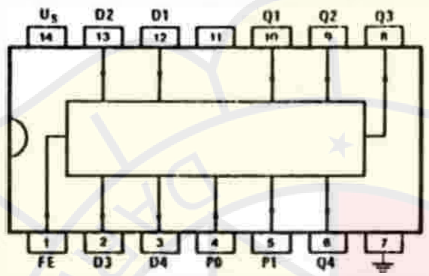
INPUT						OUT
FE1	FE2	D	C	B	A	Q=L
H	X	X	X	X	X	–
X	H	X	X	X	X	–
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
.	.	.	.	.	.	.
L	L	H	H	H	L	14
L	L	H	H	H	H	15

74159	Type		Manufact.	Bauf.	P_{typ}	t_p A,B,C,D→Q		t_p A,B,C,D→Q		
T_U = 0...70°C	-25...85°C	-55...125°C			mW					
ND 74159			Na	6a	170	24		30		
SN 74159 J		SN 54159 J	Ti	6b	170	24	23	30	30	
SN 74159 N		SN 54159 N	Ti	6a	170	24	23	30	30	
SN 74159 W		SN 54159 W	Ti	10b	170	24	23	30	30	
74159	54159		Sa	6a	170	24	23	30	30	

74278

4 bit cascadable priority register

Pin | FE
FE PO | 7 8 5



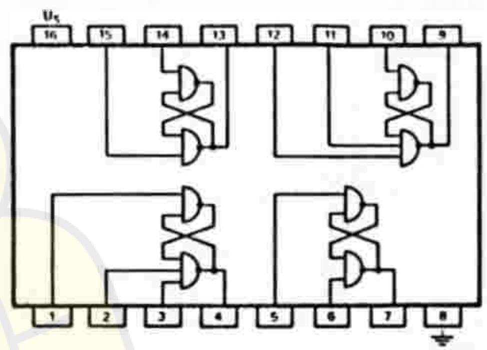
INPUT						OUTPUT				
P0	FE	D1	D2	D3	D4	Q1	Q2	Q3	Q4	P1
L	H	L	L	L	L	L	L	L	L	L
L	H	H	X	X	X	H	L	L	L	H
L	H	L	H	X	X	L	H	L	L	H
L	H	L	L	H	X	L	L	H	L	H
L	H	L	L	L	H	L	L	L	H	H
L	L	X	X	X	X				*	
H	L	X	X	X	X	L	L	L	L	H
H	H	data → register				L	L	L	L	H

* no change

74278	Type		Manufact.	θ	P_{typ}	t_{PD} D→Q		t_{PD} FE→Q		Bem. / Note
T_U = 0...70°C / 10...75°C	T_U = −25...85°C / 0...−40...85°C	T_U = −55...125°C		Bauf. 3	mW					MHz / V
SN 74278 J		SN 54278 J	[illegible]	[illegible]	275	[illegible]	[illegible]	[illegible]	[illegible]	
SN 74278 N		SN 54278 N	[illegible]	[illegible]	275	[illegible]	[illegible]	[illegible]	[illegible]	
SN 74278 W		SN 54278 W	[illegible]	[illegible]	275	[illegible]	[illegible]	[illegible]	[illegible]	
74278			[illegible]	[illegible]	275	[illegible]	[illegible]	[illegible]	[illegible]	

74279

4 RS flip flops



74279	Type		Manufact.	θ	P_{typ}	t_{PD} R→Q	t_{PD} S→Q		Bem. / Note
T_U = 0...70°C / 10...75°C	T_U = −25...85°C / 0...−40...85°C	T_U = −55...125°C		Bauf. 3	mW				MHz / V
MD 74279			[illegible]	[illegible]	[illegible]	15	[illegible]	12	
N 74279 B		S 54279 B	[illegible]	[illegible]	[illegible]	15	[illegible]	12	
N 74279 F		S 54279 F	[illegible]	[illegible]	[illegible]	15	[illegible]	12	
N 74279 W		S 54279 W	[illegible]	[illegible]	[illegible]	15	[illegible]	12	
SN 74279 J		SN 54279 J	[illegible]	[illegible]	[illegible]	15	[illegible]	12	
SN 74279 N	SN 84279 N	SN 54279 N	[illegible]	[illegible]	[illegible]	15	[illegible]	12	
SN 74279 W		SN 54279 W	[illegible]	[illegible]	[illegible]	15	[illegible]	12	
74279			[illegible]	[illegible]	[illegible]	15	[illegible]	12	
LS									
SN 74LS279 J		SN 54LS279 J	[illegible]	[illegible]	10			12	
SN 74LS279 N		SN 54LS279 N	[illegible]	[illegible]	10			12	
SN 74LS279 W		SN 54LS279 W	[illegible]	[illegible]	10			12	
9LS279 DC		9LS279 DM	[illegible]	[illegible]	[illegible]	0.27			
9LS279 FC		9LS279 FM	[illegible]	[illegible]	[illegible]	0.27			
9LS279 PC			[illegible]	[illegible]	[illegible]	0.27			

CD4017B, CD4022B Types

CMOS Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4017B—Decade Counter with
10 Decoded Outputs

CD4022B—Octal Counter with
8 Decoded Outputs

The RCA-CD4017B and CD4022B are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high-speed operation, 2-input decode-gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017B or every 8 clock input cycles in the CD4022B and is used to ripple-clock the succeeding device in a multi-device counting chain.

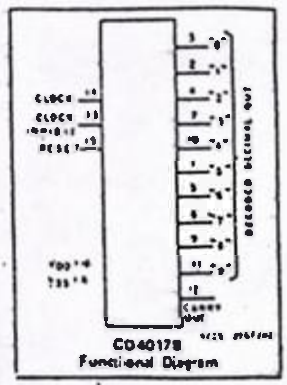
Features:

- Fully static operation
- Medium-speed operation—
  10 MHz (typ.) at V_{DD} = 10 V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

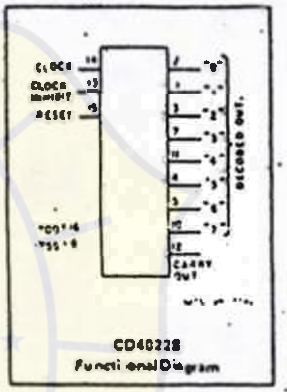
Applications:

- Decade counter/decimal decode display (CD4017B)
- Binary counter/decoder
- Frequency division
- Counter control/timers
- Divide-by-N counting
- For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"

The CD4017B and CD4022B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4017B
Functional Diagram



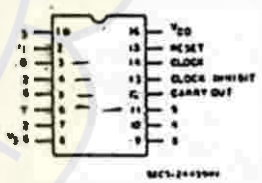
CD4022B
Functional Diagram

RECOMMENDED OPERATING CONDITIONS

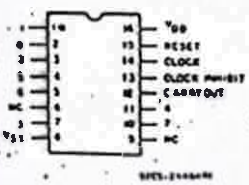
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Clock Input Frequency, f_{CL}	5	—	2.5	MHz
	10	—	5	
	15	—	5.5	
Clock Pulse Width, t_{WI}	5	200	—	ns
	10	90	—	
	15	60	—	
Clock Rise & Fall Time, t_{rCL}, t_{fCL}	5	UNLIMITED*		
	10			
	15			
Clock Inhibit Setup Time, t_s	5	230	—	ns
	10	100	—	
	15	70	—	
Reset Pulse Width, t_{RW}	5	260	—	ns
	10	110	—	
	15	60	—	
Reset Removal Time, t_{rem}	5	400	—	ns
	10	280	—	
	15	150	—	

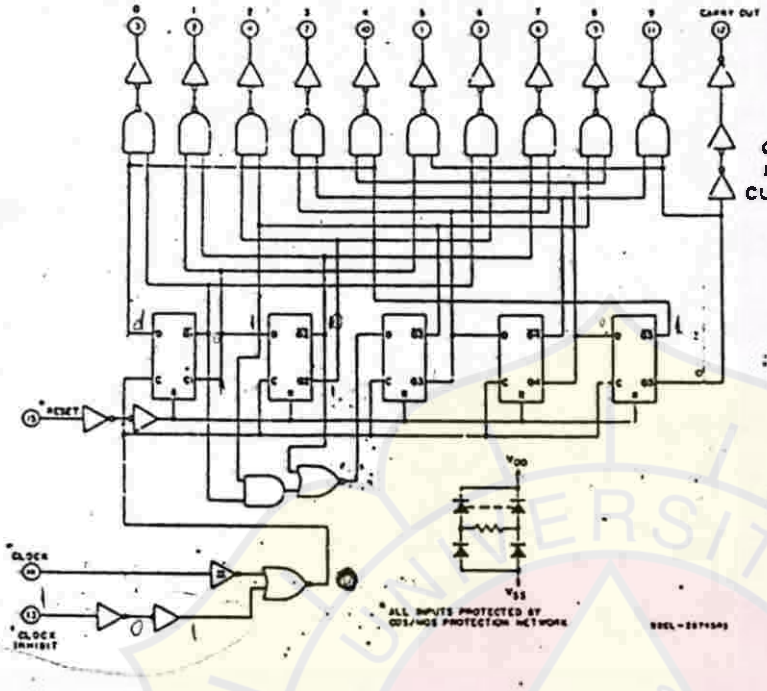
*Only if Pin 14 is used as the clock input. If Pin 13 is used as the clock input and Pin 14 is tied high (for advancing count on negative transition of the clock), rise and fall time should be ≤5 μs.



TOP VIEW
CD4017B
TERMINAL DIAGRAM



TOP VIEW
NC = no connection
CD4022B
TERMINAL DIAGRAM



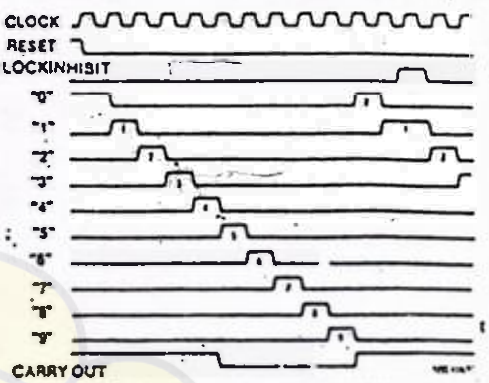


Fig. 2 – Timing diagram for CD4017B.

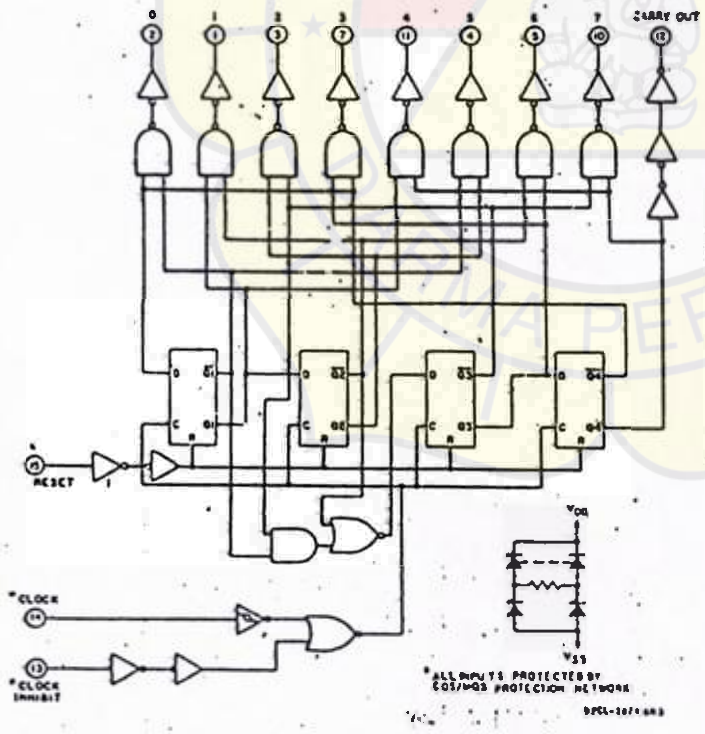


Fig. 3 – Logic diagram for CD4022B.

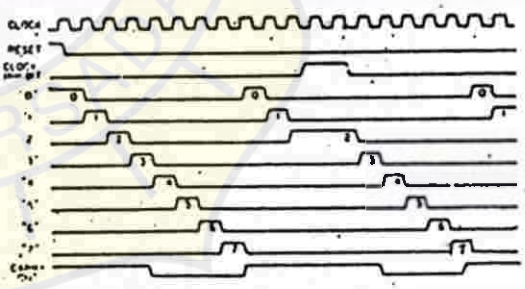


Fig. 4 – Timing diagram for CD4022B.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

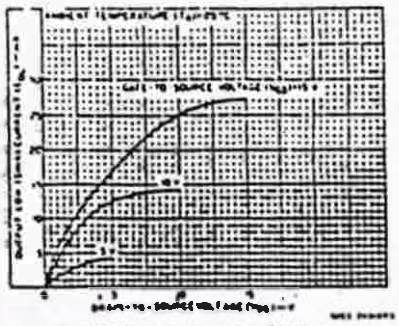


Fig. 5— Typical output low (sink) current characteristics.

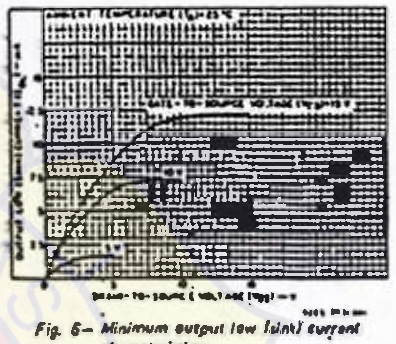


Fig. 6— Minimum output low (sink) current characteristics.

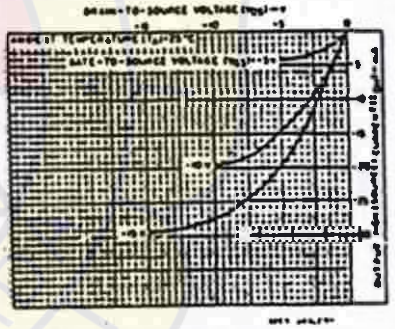


Fig. 7— Typical output high (source) current characteristics.

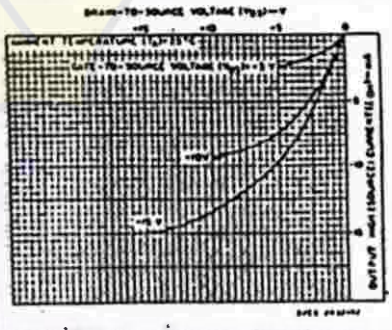


Fig. 8— Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H, Packages Values at -40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	-	0,5	5	5	5	150	150	-	0.04	5	µA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage, Low-Level, V_{OL} Max.		0,5	5	0.05				-	0	0.05	V
		0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High Level, V_{OH} Min.	-	0,5	5	4.95				4.95	5	-	
		0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage V_{IL} Max.	0.5,4.5	-	5	1.5				-	-	1.5	V
	1,9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	-	5	3.5				3.5	-	-	
	1,9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I_{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	µA

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CLOCKED OPERATION					
Propagation Delay Time, t_{PHL}, t_{PLH} Decode Out	5	–	325	650	ns
	10	–	135	270	
	15	–	85	170	
Carry Out	5	–	300	600	
	10	–	125	250	
	15	–	80	160	
Transition Time, t_{THL}, t_{TLH} Carry Out or Decode Out Line	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency, f_{CL}*	5	2.5	5	–	MHz
	10	5	10	–	
	15	5.5	11	–	
Minimum Clock Pulse Width, t_W	5	–	100	200	ns
	10	–	45	90	
	15	–	30	60	
Clock Rise or Fall Time, t_rCL, t_fCL	5, 10, 15	UNLIMITED			
Minimum Clock Inhibit to Clock Setup Time, t_s	5	–	115	230	ns
	10	–	50	100	
	15	–	35	70	
Input Capacitance, C_{IN}	Any Input	–	5	–	pF
RESET OPERATION					
Propagation Delay Time, t_{PHL}, t_{PLH} Carry Out or Decode Out Lines	5	–	265	530	ns
	10	–	115	230	
	15	–	85	170	
Minimum Reset Pulse Width, t_W	5	–	130	260	ns
	10	–	55	110	
	15	–	30	60	
Minimum Reset Removal Time	5	–	200	400	ns
	10	–	140	280	
	15	–	75	150	

* Measured with respect to carry output line.

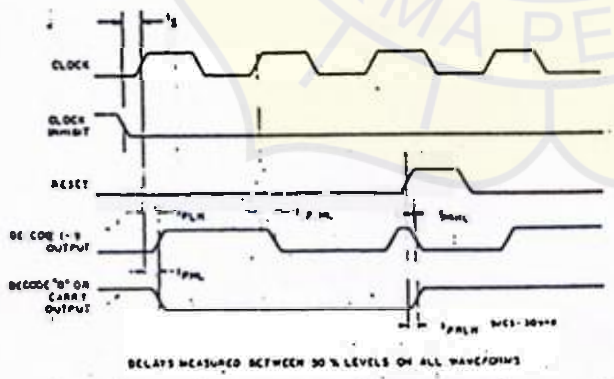


Fig. 9 – Propagation delay, setup, and hold time waveforms.

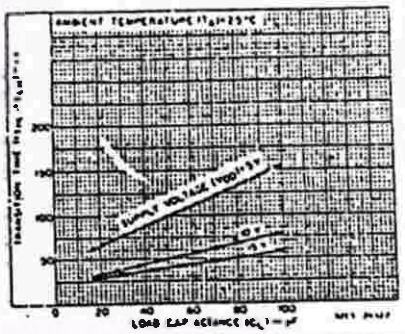


Fig. 10 – Typical transition time as a function of load capacitance.

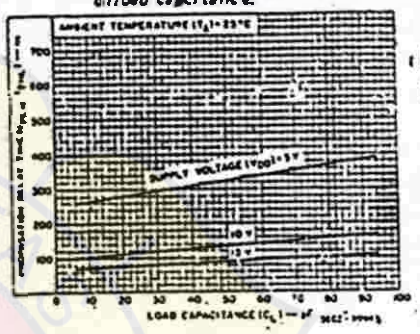


Fig. 11 – Typical propagation delay time as a function of load capacitance (clock to decode output).

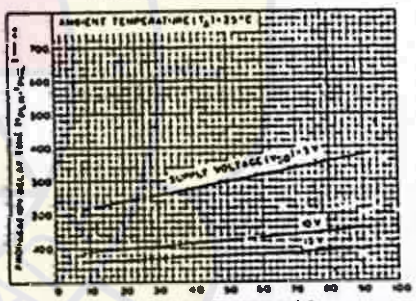


Fig. 12 – Typical propagation delay time as a function of load capacitance (clock to carry-out).

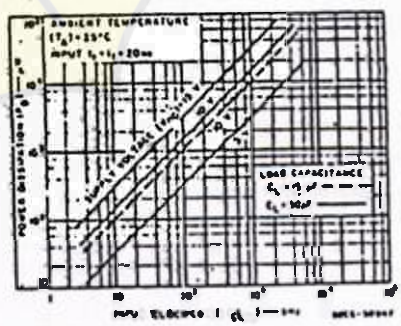


Fig. 13 – Typical dynamic power dissipation as a function of clock input frequency.

MITEL

ISO²-CMOS MT8870B/MT8870B-1
Integrated DTMF Receiver

9161-002-051-NA ISSUE 2 December 1987

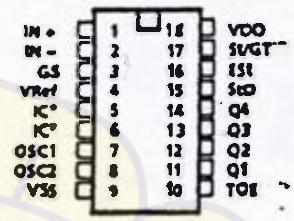
Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

Applications

- Receiver System for British Telecom (BT) or CEPT Spec (MT8870B-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers

Pin Connections



* Connected to VSS

Ordering Information

MT8870B/MT8870B-1 Plastic DIP
MT8870C/MT8870C-1 Cerdip
-40°C to +85°C

Description

The MT8870B/MT8870B-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

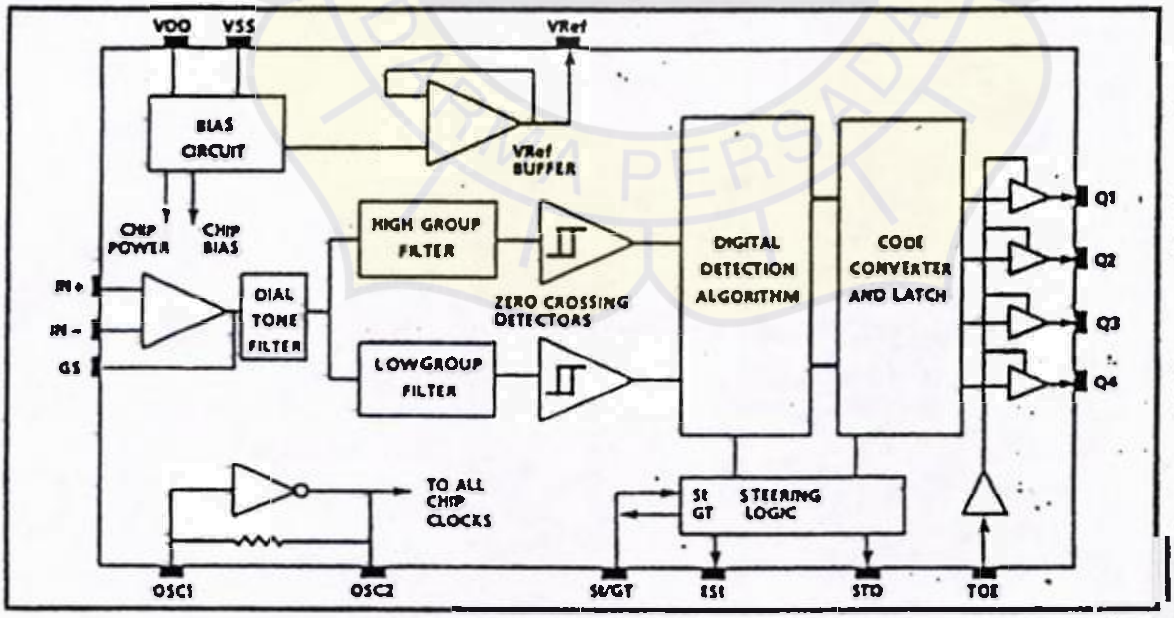


Figure 1- Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}			6	V
2	Voltage on any pin		V_{SS} -0.3	V_{DD} +0.3	V
3	Current at any pin (other than supply)			10	mA
4	Operating temperature	T_A	-40	+85	°C
5	Storage temperature		-65	+150	°C
6	Package power dissipation			1000	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

†Derate above 75°C at 16 mW/°C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	Positive Supply Voltages	V_{DD}		5		V	V_{SS} = 0V
2	Oscillator Clock Frequency	fc		3.579545		MHz	
3	Oscillator Frequency Tolerance	Δfc		±0.1		%	

†Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD} = 5.0V ±5%, V_{SS} = 0V. Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ†	Max	Units	Test Conditions
1	SUPPLY	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_D		15	45	mW	f = 3.58MHz; V_{DD} = 5V
4	INPUTS	High level input	V_{IH}	3.5			V	
5		Low level input voltage	V_{IL}			1.5	V	
6		Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
7		Pull-up (source) current	I_{SO}		7.5	15	μA	TOE (pin 10) = 0V
8		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@1kHz
9		Steering threshold voltage	V_{TSt}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			V_{SS} +0.03	V	No load
11		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
12		Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4V
13		Output high(source) current	I_{OH}	0.4	0.8		mA	V_{OUT} =4.6V
14		V_{Ref} output voltage	V_{Ref}	2.4		2.7	V	No load
15		V_{Ref} output resistance	R_{OR}		10		kΩ	

†Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

Operating Characteristics'- Voltages are with respect to ground (V_{SS}) unless otherwise stated
Gain Setting Amplifier

	Characteristics	Sym	Min	Typ'	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power supply rejection	PSRR		60		dB	1KHz
5	Common mode rejection	CMRR		60		dB	$-3.0V \leq V_{IN} \leq 3.0V$
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth	f_c		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \geq 100K\Omega$ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
0	Maximum resistive load (GS)	R_L		50		KΩ	
1	Common mode range	V_{CM}		3.0		V_{pp}	No Load

= 5 V, ½ 0 V, T_A = 2 5°C
>cal figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

'8870B AC Electrical Characteristics' - Voltages are with respect to ground (V_{SS}) unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Notes
SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-29		1	dBm	1,2,3,5,6,9
			27.5			mV_{RMS}	1,2,3,5,6,9
					+ 1	dBm	1,2,3,5,6,9
					869	mV_{RMS}	1,2,3,5,6,9
	Positive twist accept			10		dB	2,3,6,9
	Negative twist accept			10		dB	2,3,6,9
	Freq. deviation accept		±1.5% ± 2Hz			Nom.	2,3,5,9
	Freq. deviation reject		±3.5%			Nom.	2,3,5,9
	Third tone tolerance			-16		dB	2,3,4,5,9
	Noise tolerance			-12		dB	2,3,4,5,7,9,10
	Dial tone tolerance			+ 22		dB	2,3,4,5,8,9,11

5 V, V_{SS} = 0, T_A = 25°C and f_C = 3.579545 MHz using test circuit shown in Figure 2

= decibels above or below a reference power of 1 mW into a 600 ohm load.
sequence consists of all DTMF tones
duration 40 m s, tone pause = 40 m s.
condition consists of nominal DTMF frequencies
tones in composite signal have equal amplitude.
pair is deviated by ±1.5% ± 2Hz.
width limited (3kHz) Gaussian noise.
reverse dial tone frequencies are (350Hz and 440Hz) ± 2%.
error rate of better than 1 in 10,000.
sured to lowest level frequency component in D T M signal.
sured to the minimum valid accept level.

MT8870B-1 AC Electrical Characteristics* - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-31			dBm	1,2,3,5,6,9
				21.8			mV_{RMS}	1,2,3,5,5.9
						+1	dBm	1,2,3,5,6,9
						869	mV_{RMS}	1,2,3,5,6,9
2		Input Signal Level Reject		-37			dBm	1,2,3,5,6,9
				10.9			mV_{RMS}	1,2,3,5,6,9
3		Positive twist accept				6	dB	2,3,6,9
4		Negative twist accept				6	dB	2,3,6,9
5		Freq. deviation accept		±1.5% ± 2Hz				2,3,5,9
6		Freq. deviation reject		±3.5%				2,3,5,9
7		Third tone tolerance		-18.5			dB	2,3,4,5,9,12
8		Noise tolerance			-12		dB	2,3,4,5,7,9,10
9		Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

* V_{DD} = 5 V, V_{SS} = 0 , T_A = 25° C and f_c = 3.579545 MHz using test circuit shown in Figure 2.

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ± 2Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 Input DTMF Tone Level at -25 dBm (-28 dBm at GS Pin) Interference Frequency Range between 480-3400 Hz.

Electrical Characteristics--Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure3
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	$\overline{t_{REC}}$	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	$\overline{t_{ID}}$	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12		µs	TOE = V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		µs	TOE = V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	RL = 10KΩ CL=50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	RL = 10KΩ CL = 50 pF
12	CLOCK	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
13		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
14		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
15		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
16		Capacitive load (OSC2)	C_{LO}			30	pF	

= 5.0V, V_{SS} = 0V, T_A = 25°C and f_C = 3.579545MHz, using test circuit shown in Figure 2

cal figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

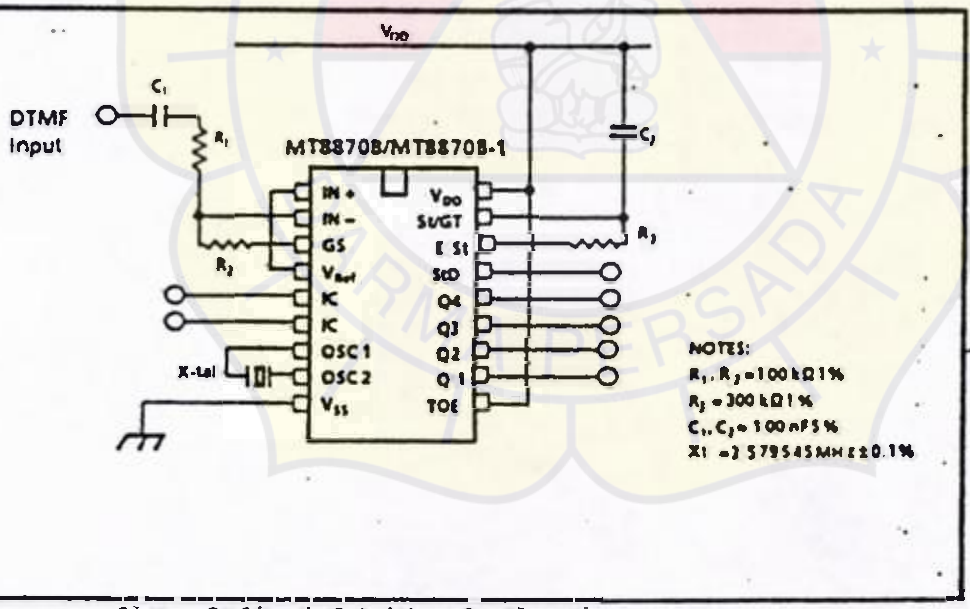


Figure 2 - Single-Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN +	Non-Inverting Op-Amp (Input).
2	IN −	Inverting Op-Amp (Input).
3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{Ref}	Reference Voltage (Output). Nominally $V_{DD}/2$ isused to bias inputs at mid-rail (see Fig.2).
5	IC	Internal Connection. Must be tied to V_{SS}.
6	IC	Internal Connection. Must be tied to V_{SS}.
7	OSC1	Clock (Input).
8	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	V_{SS}	Negative Power Supply (Input).
10	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE islogic low, the data outputs are high impedance.
15	StD	Delayed Steering (Output).Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}
16	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply (Input).

ctional Description

MT8870B/MT8870B-1 monolithic DTMF receiver rs small size, low power consumption and high formance. Its architecture consists of a bandsplit r section, which separates the high and low up tones, followed by a digital counting section ch verifies the frequency and duration of the ived tones before passing the corresponding e to the output bus.

er Section

aration of the low group and high group tones chieved by applying the DTMF signal to the uts of two sixth-order switched capacitor ndpass filters, the bandwidths of which respond to the low and high group frequencies. filter section also incorporates notches at 350 440 Hz for exceptional dial tone rejection.(see ure 4). Each filter output is followed by a single ler switched capacitor filter section which oths the signals prior to limiting. Limiting is formed by high-gain comparators which are nded with hysteresis to prevent detection of wanted low-level signals. The outputs of the nparators provide full rail logic swings at the quencies of the incoming DTMF signals.

coder Section

lowing the filter section is a decoder employing gital counting techniques to determine the quencies of the incoming tones and to verify that ty correspond to standard DTMF frequencies. A nplex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 5) to rise as the capacitor discharges. Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate

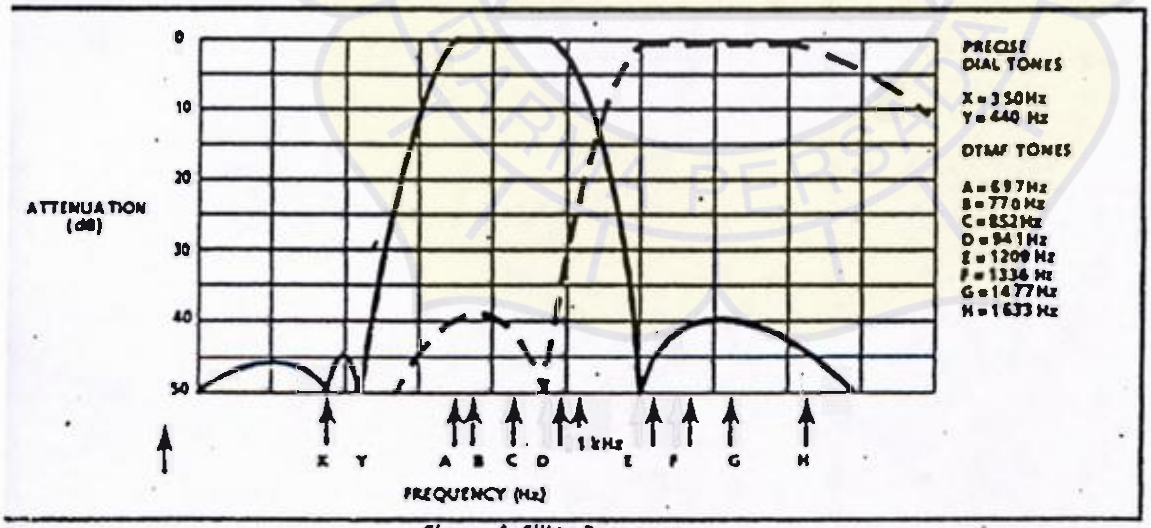


Figure 4- Filter Response

the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Figure 5 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see Figure 3) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone dropouts are required. Design information for guard time adjustment is shown in Figure 6.

Differential Input Configuration

The input arrangement of the MT8870B/MT8870B-1 provides a differential-input operational amplifier as well as a bias source(V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 2 with the op-amp connected for unity gain and V_{Ref} biasing the input at $\frac{1}{2}V_{DD}$. Figure 7 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_F.

F_{LOW}	F_{HIGH}	NO.	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
·	·	ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE

Table 1. Functional Decode Table

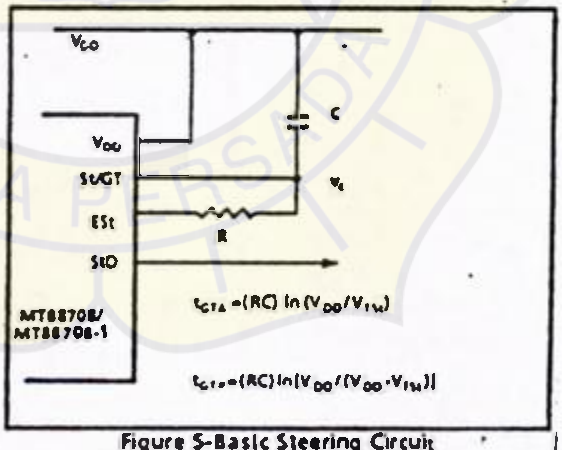


Figure 5-Basic Steering Circuit

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is

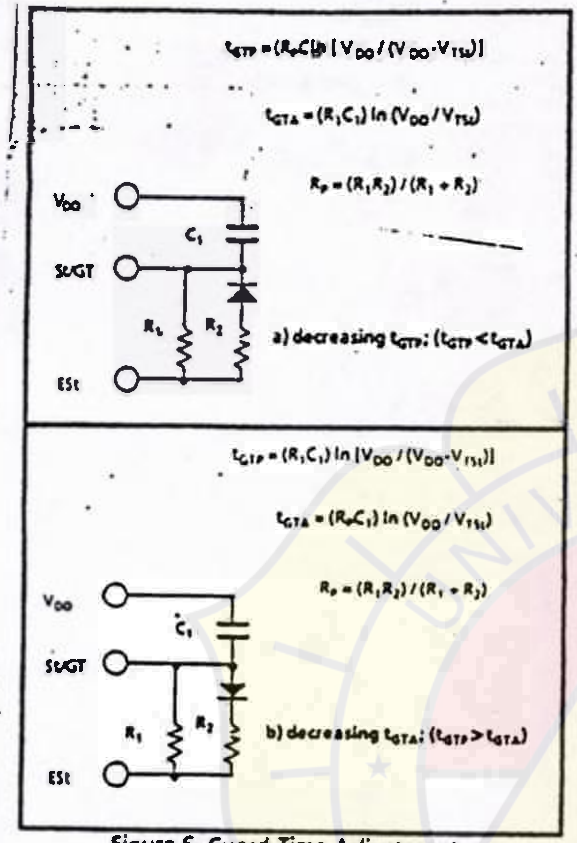


Figure 6- Guard Time Adjustment

normally connected as shown in Figure 2 (Single Ended Input Configuration). However, it is possible to configure several MT8870B/MT8870B-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 8 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie; precision balancing capacitors are not required.

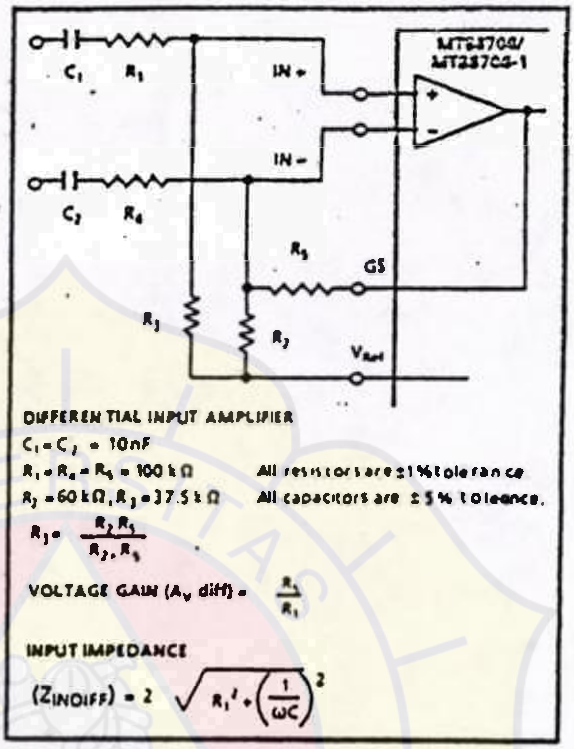


Figure7- Differential Input Configuration

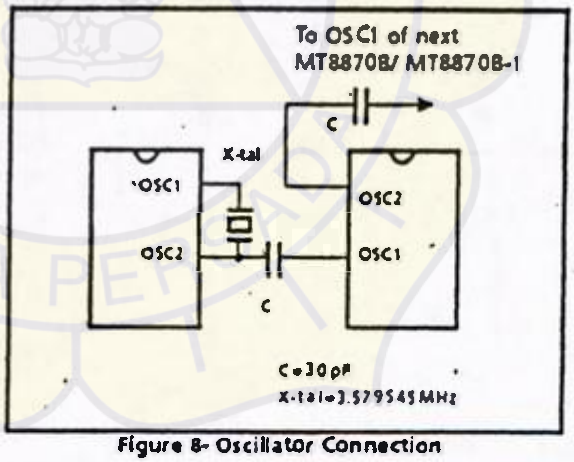


Figure 8- Oscillator Connection

APPLICATION

RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 10 illustrates the use of MT8870B-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R_1 and R_2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870B-1. As shown in the diagram, the component values of R_3 and C_2 are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 9.

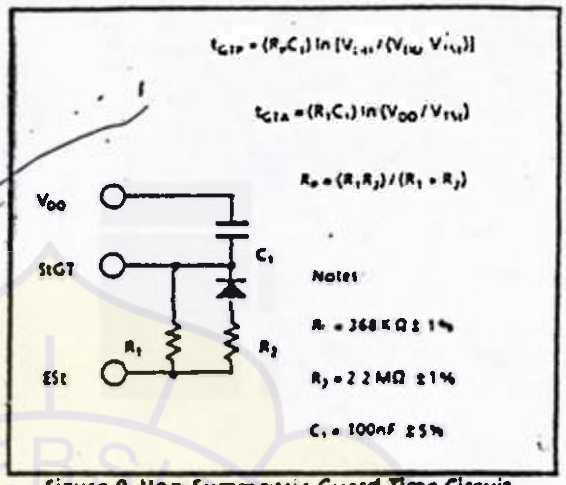


Figure 9-Non-Symmetric Guard Time Circuit

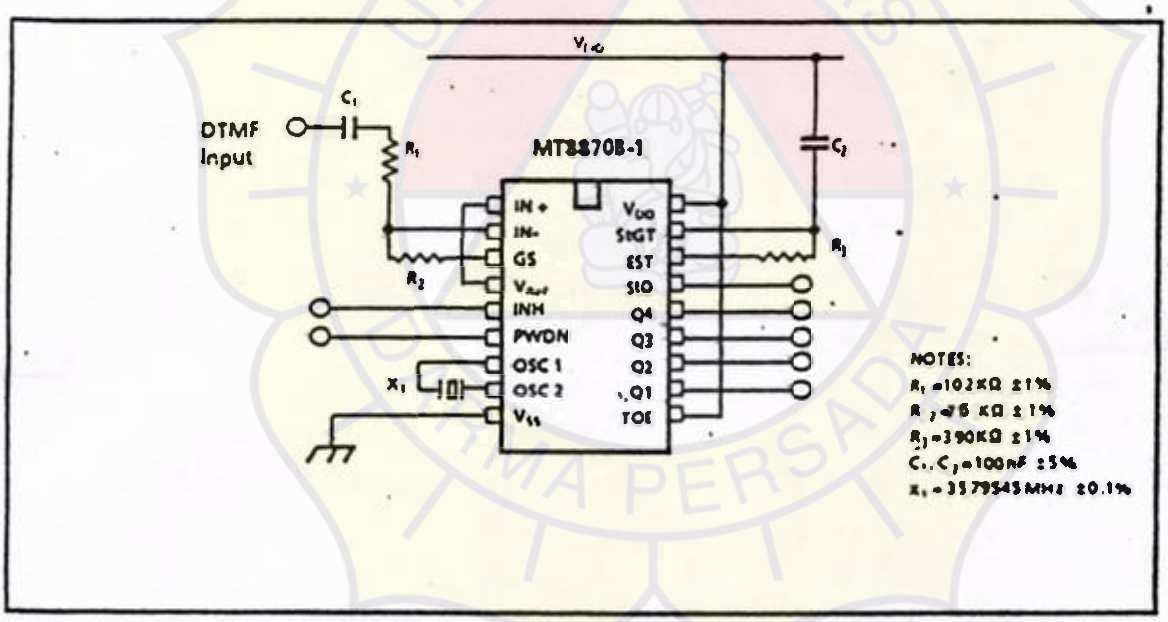


Figure 10 - Single-Ended Input Configuration for BT or CEPT Spec